Code No: R32052 **R10** **Set No: 1**

III B.Tech. II Semester Regular Examinations, April/May -2013

COMPUTER ARCHITECTURE

(Computer Science and Engineering)

Time: 3 Hours **Max Marks: 75**

Answer any FIVE Questions

All Questions carry equal marks

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1. (a) Briefly discuss the five generations of electronic computers.
   (b) What are the two approaches to parallel programming? Explain them with necessary diagrams.

2. (a) What is a virtual machine? Discuss protection via virtual machine
   (b) Explain the basic memory hierarchy.

3. (a) Discuss the locality property for hierarchical memory technology.
   (b) Explain in detail the characteristics of a typical CISC processor.

4. (a) Discuss the two models of linear pipeline units with necessary diagrams.
   (b) What are collision vectors? Describe their role in scheduling.

5. Explain crossbar networks. Give the schematic design of a cross point switch in a crossbar network. Discuss the limitations of crossbar.

6. (a) Describe the cache coherence problems in data sharing and in process migration.
   (b) What is a virtual channel? Explain its role in dead lock avoidance.

7. Discuss in detail the four categories of inter processor communication in CM-5 system.

8. (a) Explain stream processing as a form of parallelism.
   (b) Write a note on Cray Line of computer systems.

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Code No: R32052 **R10** **Set No: 2**

III B.Tech. II Semester Regular Examinations, April/May -2013

COMPUTER ARCHITECTURE

(Computer Science and Engineering)

Time: 3 Hours **Max Marks: 75**

Answer any FIVE Questions

All Questions carry equal marks

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1. (a) Explain the elements of a modern computer system in the context of parallel processing.
   (b) Differentiate between UMA, NUMA, COMA models.

2. Discuss advanced optimizations of cache performance.

3. (a) Discuss the coherence property for hierarchical memory technology.
   (b) Explain in detail the characteristics of a typical RISC processor.

4. Describe scheduling events in a nonlinear pipeline. How to achieve collision-free scheduling?

5. (a) Discuss the hot-spot problem.
   (b) Explain various vector instruction types with necessary diagrams.

6. (a) Describe adaptive routing on a 2D mesh-connected multicomputer.
   (b) Briefly explain snoopy bus protocols.

7. Describe the functional architectures of the control processors and the processing nodes in the CM-5.

8. (a) Compare and contrast structural parallelism with instructional level parallelism.
   (b) Write a detail note on stream processing.

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Code No: R32052 **R10** **Set No: 3**

III B.Tech. II Semester Regular Examinations, April/May -2013

COMPUTER ARCHITECTURE

(Computer Science and Engineering)

Time: 3 Hours **Max Marks: 75**

Answer any FIVE Questions

All Questions carry equal marks

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1. (a) Briefly discuss the evolution of computer architecture.
   (b) Explain SIMD computer. Give its machine model and operational model.

2. (a) What is meant by virtual memory? Discuss protection via virtual memory.
   (b) Explain the significance of cache memory in a system. How to measure the performance of cache memory?

3. Explain the design space for processors and also instruction set architectures.

4. (a) Differentiate between asynchronous and synchronous models of linear pipeline units.
   (b) Discuss reservation and latency analysis of dynamic pipeline.

5. Discuss in detail routing in omega networks and routing in butterfly networks.

6. (a) Describe cache events and actions.
   (b) Explain E-cube routing on Hypercube.

7. (a) Discuss the two SIMD computer models.
   (b) Write about hyper cube routers in CM-2.

8. Write matrix multiplication algorithm. Can it be parallelized? Justify your answer by applying suitable form of parallelism.

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Code No: R32052 **R10** **Set No: 4**

III B.Tech. II Semester Regular Examinations, April/May -2013

COMPUTER ARCHITECTURE

(Computer Science and Engineering)

Time: 3 Hours **Max Marks: 75**

Answer any FIVE Questions

All Questions carry equal marks

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1. (a) Discuss the system attributes to performance.
   (b) Give the architecture of a vector super computer and explain it briefly.

2. (a) Discuss the characteristics of memory types in basic memory hierarchy.
   (b) Explain any three advanced optimization approaches for cache memory.

3. (a) Compare and contrast general CISC processor with RISC processor
   (b) Describe the inclusion property and coherence property for hierarchical memory.

4. (a) Explain the asynchronous model of linear pipeline unit.
   (b) Discuss pipeline schedule optimization based on MAL.

5. (a) Elaborate on hierarchical bus systems.
   (b) Discuss Cray Y-MP 816 system organization.

6. Discuss various issues pertaining to multicast routing algorithms on a mesh-connected computer.

7. (a) Discuss parallel prefix operation on the CM-5.
   (b) Give the architecture of CM-2 and explain.

8. Describe in detail parallel systems aspects of Cray line of computer systems.

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