Code No: V3119 **R07** **Set No: 1**

III B.Tech. I Semester Supplementary Examinations, April/May - 2013

COMPUTER ORGANIZATION

(Common to ECE, EIE)

Time: 3 Hours **Max Marks: 80**

Answer any FIVE Questions

All Questions carry equal marks

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1. a) Explain about various buses such as internal, external, I/O, system, address, data, synchronous and asynchronous. What do you mean by bus width?
   b) Explain sign magnitude and 2's complement approaches for representing the fixed point numbers. Why 2's complement is preferable.

2. a) Describe various arithmetic and logical instruction set operations.
   b) Explain the instruction execution characteristics of RISC processors.

3. a) List and explain the functions of control unit.
   b) Explain the functioning of micro sequencer with example.

4. a) What is overflow and underflow? What is the reason? If the computer is considered as infinite system do we still have these problems?
   b) Explain about the longhand division of binary integers.

5. a) Explain the organization of a 1K x 1 Memory with a neat sketch.
   b) What is Virtual Memory? What are the issues behind the usage of this technique?

6. Discuss three possible techniques for I/O operations with merits and demerits of each.

7. a) What is pipelining? Explain four segment pipelining.
   b) Explain array processors.

8. a) Explain multiport memory organization with a neat sketch.
   b) What is cache coherence problem? Discuss various cache coherence approaches.

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Code No: V3119 **R07** **Set No: 2**

III B.Tech. I Semester Supplementary Examinations, April/May - 2013

COMPUTER ORGANIZATION

(Common to ECE, EIE)

Time: 3 Hours **Max Marks: 80**

Answer any FIVE Questions

All Questions carry equal marks

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1. a) Write about the interconnection structure design of a computer.
   b) List various registers in a computer along with their purpose.

2. a) What are register transfer logic languages? Explain few RTL statement for branching with their actual functioning.
   b) Explain about stack organization used in processors. What do you understand by register stack and memory stack?

3. a) What are the design goals for a designer while deciding a hardwired or micro-programmed control unit for a CPU.
   b) Explain about microinstruction format.

4. a) Explain Booth's algorithm with its theoretical basis.
   b) Multiply 10111 with 10011 using booths algorithm.

5. a) A computer uses RAM chips of 1024 x 1 capacity.
      (i) How many chips are needed and how should their address lines be connected to provide a memory capacity of 1024 bytes?
      (ii) How many chips are needed to provide a memory capacity of 16Kbytes?
   b) What is Redundant Array of Inexpensive Discs? What are the advantages of using this kind of systems?

6. a) Explain programmed I/O in detail.
   b) What are the different issues behind serial communication? Explain.

7. a) Differentiate between two-stage and four-stage pipelines.
   b) Explain SIMD and MIMD processors in detail.

8. a) Explain the working of 8 x 8 Omega Switching network..
   b) Discuss different approaches to vector computation.

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R07 **Set No: 3**

Code No: V3119

III B.Tech. I Semester Supplementary Examinations, April/May - 2013

COMPUTER ORGANIZATION

(Common to ECE, EIE)

Time: 3 Hours **Max Marks: 80**

Answer any FIVE Questions

All Questions carry equal marks

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1. a) What are the different performance measures used to represent a computer systems Performance?
   b) Give means to identify whether or not an overflow has occurred in 2's complement addition or subtraction operations. Take one example for each possible situation and explain. Assume 4 bit registers.

2. Design a circuit to increment, decrement, complement and clear a 4 bit register using RS flip-flops. Explain the control logic.

3. a) Explain branch control logic in microinstruction sequencing with variable address format.
   b) Differentiate between horizontal and vertical micro instructions.

4. Write an algorithm to subtract binary numbers represented in normalized floating point mode with base 2 for exponent

5. a) Write about address translation in paging.
   b) What are the advantages and disadvantages of using the technique of Paged Segmentation?

6. a) Discuss elaborately data organization and formatting of magnetic disk.
   b) Define disk access time, seek time and rotational latency.

7. a) Discuss the demerits of pipelined processing.
   b) Write about RISC pipelining with regular instructions.

8. a) Differentiate between high-level and low-level parallelism.
   b) Discuss the Flynn's classification of parallel processor systems.
   c) Explain different MIMD interconnection topologies.

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Code No: V3119 **R07** **Set No: 4**

III B.Tech. I Semester Supplementary Examinations, April/May - 2013

COMPUTER ORGANIZATION

(Common to ECE, EIE)

Time: 3 Hours **Max Marks: 80**

Answer any FIVE Questions

All Questions carry equal marks

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1. a) Explain the normalized floating point representation in detail.
   b) With an example, explain Cyclic Redundancy Check.

2. a) Explain about instruction, fetch, and decode cycles for a memory reference instruction. Draw a flow chart to explain the same. Indicate clearly where and which processor registers come into picture.
   b) Explain how X=(A+B)/(A-B) is evaluated in a stack based computer?

3. a) Explain the organization of control memory.
   b) Explain the functioning of micro-programmed control unit.

4. a) How many bits are needed to store the result of addition, subtraction, multiplication and division of two n-bit unsigned numbers. Prove.
   b) Draw a flowchart to explain how addition and subtraction of two fixed point numbers can be done? Also, draw a circuit using full adders for the same.

5. What are the different types of Mapping Techniques used in the usage of Cache Memory? Explain.

6. a) Explain interrupt initiated I/O in detail.
   b) Explain bit oriented and character oriented protocols in serial communication.

7. a) Show space-time diagram for pipeline. Explain with an example.
   b) Explain vector processing.

8. a) Explain the functioning of Binary Tree network with 2 x 2 Switches. Show a neat sketch.
   b) Give a summary of arithmetic and logical operations that are defined for the vector architecture.

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