Code No: R22054 **R10** SET - 1

**II B. Tech II Semester, Supplementary Examinations, Dec – 2012**
**COMPUTER ORGANIZATION**
(Com. to CSE, ECC)

Time: 3 hours Max. Marks: 75

Answer any **FIVE** Questions
All Questions carry **Equal** Marks
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1. a) Explain the assembly process for assembly language programs.
   b) Explain the various instruction formats of the 8085 micro processor.

2. Explain about memory sub system organization and interfacing.

3. Explain the operation of toll Booth controller.

4. Draw and explain the register section for a relatively simple CPU.

5. a) Explain about BCD adder.
   b) Explain about floating point number representation.

6. a) Explain about associative memory in detail.
   b) Compare write-through and write-back.

7. Explain DMA mode of data transfer.

8. a) Explain about branch conflicts.
   b) Explain about routing on multistage inter connection Networks.
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Code No: R22054 **R10** SET - 2

**II B. Tech II Semester, Supplementary Examinations, Dec – 2012**
**COMPUTER ORGANIZATION**
(Com. to CSE, ECC)

Time: 3 hours Max. Marks: 75

Answer any **FIVE** Questions
All Questions carry **Equal** Marks
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1. a) Explain about the various addressing modes.
   b) Explain about instruction set for a relatively simple CPU.

2. a) Construct an 8×4 memory subsystem from two 8×2 ROM chips.
   b) Write about multi byte Data Organization.

3. a) Explain the VHDL design with a high level of abstraction.
   b) Draw the state table for Module '6' counter.

4. a) Draw and explain a relatively simple CPU.
   b) Explain the generic micro sequencer organization.

5. a) Explain the RTL code for the shift-add algorithm.
   b) Explain the hardware to implement BCD addition and subtraction.

6. Explain cache memory with Associative mapping.

7. a) Write about types of interrupts.
   b) Explain about DMA transfer modes.

8. a) Compare RISC Vs. CISC.
   b) Explain about SIMD organization.
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Code No: R22054 **R10** SET - 3

**II B. Tech II Semester, Supplementary Examinations, Dec – 2012**
**COMPUTER ORGANIZATION**
(Com. to CSE, ECC)

Time: 3 hours Max. Marks: 75

Answer any **FIVE** Questions
All Questions carry **Equal** Marks
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1. a) Explain the program control instruction of the 8085 Micro processor.
   b) Explain the instruction set Architecture Design.

2. a) Explain the memory subsystem details in relatively simple computer.
   b) What are the various types of ROM chips.

3. a) Explain the implementation of the data transfer
   $\alpha : X < -Y, Y < -Z$
   b) Explain the operation of D-flip-flop.

4. a) Explain the generic bidirectional data pin.
   b) Explain micro sequencer for the relatively simple CPU with micro subroutines.

5. a) Explain hardware implementation of Booths multiplication algorithm.
   b) Explain about floating point numbers representation.

6. Explain in detail about virtual memory.

7. a) Write about source-initiated data transfer.
   b) Explain about Serial communication.

8. a) Compare RISC with CISC.
   b) Explain multi processor system topologies.
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Code No: R22054 **R10** SET - 4

**II B. Tech II Semester, Supplementary Examinations, Dec – 2012**
**COMPUTER ORGANIZATION**
(Com. to CSE, ECC)

Time: 3 hours Max. Marks: 75

Answer any **FIVE** Questions
All Questions carry **Equal** Marks
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1. a) Write 8085 assembly language program to find the sum of first 'n' numbers.
   b) Explain the various flags in 8085 micro processor.

2. a) Explain the CPU internal organization.
   b) Show how the following values are stored in memory in big endian and little endian formats. Each value starts at location 22H.
   i) 0927H ii) 12345678H

3. Explain the working of modulo '6' counter.

4. a) Show the logic needed to generate the control signals for registers PC, DR, TR and IR of the relatively simple CPU.
   b) Draw and explain the generic micro instruction format.

5. a) Explain the hardware implementation of the shift-add multiplication algorithm.
   b) Write about Wallace trees.

6. a) Explain cache memory with set associative map.
   b) Write about cache performance.

7. a) Describe destination initiated data transfer.
   b) Explain I/O processor mode of data transfer.

8. a) Explain about RISC instruction set.
   b) Explain MIMD system architectures.
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