Code No: V3119 **R07** **Set No: 1**

III B.Tech. I Semester Supplementary Examinations, November/December - 2012

COMPUTER ORGANIZATION

(Common to Electronics and Communication Engineering & Electronics and Instrumentation Engineering)

Time: 3 Hours **Max Marks: 80**

Answer any FIVE Questions

All Questions carry equal marks

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1. Explain the computer structure with and its component and their Functions in detail [16]

2. (a) Explain about stack organization used in processors. What do you understand by register stack and memory stack?
   (b) Explain how X=(A*B)/(A+B) is evaluated in a stack based computer. [10+6]

3. (a) How do we reduce number of microinstructions. What are micro-subroutines?
   (b) Hardwired control unit is faster than micro-programmed control unit. Justify this statement. [8+8]

4. Explain floating point arithmetic operations in detail with algorithm. [16]

5. (a) What is the functioning of a Flash Memory? Explain
   (b) Describe in words by means of a block diagram how multiple matched words can be read out from an associative memory [8+8]

6. Explain the following in detail
   (a) Programmed I/O
   (b) Interrupt- initiated I/O
   (c) Direct Memory Access (DMA) [5+5+6]

7. (a) What is pipeline? Explain with suitable diagram.
   (b) Explain instruction pipeline with suitable diagram. [8+8]

8. Explain the Interprocessor Arbitration and cache coherence in detail. [16]

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Code No: V3119 **R07** **Set No: 2**

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Time: 3 Hours **Max Marks: 80**

Answer any FIVE Questions

All Questions carry equal marks

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1. Discuss about the various generations of computers in detailed [16]

2. (a) Design a circuit transferring data from a 4bit register which uses D flip-flops to another register which employs RS flip-flops.
   (b) What are the register transfer logic languages? Explain few RTL statement for branching with their actual functioning. [8+8]

3. (a) How do you map micro-operation to a micro instruction address?.
   (b) Explain the difference between hardwired control and micro programmed control. Is it possible to have a hardwired control associated with a control memory? [8+8]

4. (a) Explain the Addition and subtraction with unsigned-magnitude.
   (b) Explain the Booth multiplication algorithm [8+8]

5. Explain the following
   i. Auxiliary memory
   ii. Associative memory
   iii. Cache memory [5+6+5]

6. (a) Explain the various peripheral devices of a computer sytem.
   (b) Discus Input-Output Interface in detail [8+8].

7. (a) Explain four segment pipelining with relevant diagram.
   (b) Explain Array processors in detailed [8+8]

8. Explain the Interprocessor communication and synchronization in detail. [16]

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Code No: V3119 **R07** **Set No: 3**

III B.Tech. I Semester Supplementary Examinations, November/December - 2012

COMPUTER ORGANIZATION

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Time: 3 Hours **Max Marks: 80**

Answer any FIVE Questions

All Questions carry equal marks

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1. (a) List and Explain the key characteristics of a computer.
   (b) Distinguish between error detection and correction codes. What do you understand by odd parity and even parity?. What is odd function and even function. To calculate odd and even parity values which functions can be used? [8+8]

2. Write about direct, indirect, register direct, register indirect, immediate, implicit, relative, index, and base address mode of addressing. Why do we need so many addressing modes? Is the instruction size influenced by the number of addressing modes which a processor supports? State whether the number of addressing modes will be more in RISC or CISC? [16]

3. (a) what is the difference between the microprocessor and a micro program? Is it possible to design a microprocessor without a micro program? Are all micro programmed computers also microprocessors? Explain.
   (b) Explain nanoinstructions and nanometry. Why do we need them? [8+8]

4. (a) What is an arithmetic processor? Explain.
   (b) Explain various decimal arithmetic operations. [8+8]

5. (a) Explain Memory hierarchy in detailed
   (b) Explain memory management hardware in detailed [8+8]

6. (a)Explain the Input-Output Processor (IOP) in detail.
   (b) Why does DMA have priority over the CPU when both request a memory transfer? [10+6]

7. Explain the following
   (a)RISC Pipeline
   (b)Array Processors. [8+8]

8. (a) Explain the characteristics of multiprocessors
   (b) Explain the functioning of Binary Tree network with 2 x 2 Switches. Show a neat diagram [8+8]

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Code No: V3119 **R07** **Set No: 4**

III B.Tech. I Semester Supplementary Examinations, November/December - 2012

COMPUTER ORGANIZATION

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Time: 3 Hours **Max Marks: 80**

Answer any FIVE Questions

All Questions carry equal marks

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1. (a) Explain the computer system with various buses and their functions with a diagram.
   (b) assume numbers are represented in 8-bit twos complement representation.Show the calculation of the following:
   i) 6+13 ii) -6 + 13 iii) 6 -13 iv) -6-13 [8+8]

2. (a) Explain about stack organization used in processors. What do you understand by register stack and memory stack?
   (b) Explain how X=(A+B)/(A-B) is evaluated in a stack based computer. [10+6]

3. (a) Support the statement Instruction Set Architecture has impact on the processors micro architecture
   (b) Explain the design of hardwired control unit with relevant diagram [8+8]

4. (a) Explain the Booth multiplication algorithm
   (b) Explain the decimal Arithmetic operations in detailed [8+8]

5. (a) Explain the Memory Hierarchy with neat diagram. [8+8]
   (b) A virtual memory has a page size of 1k words. There are eight pages and four blocks. The associative page table contains the following entries:

pages	0	1	4	6
Blocks	3	1	2	0

   Make a list of all virtual addresses (in decimal) that will cause a page fault if used by the CPU [8+8]

6. Explain various asynchronous data transfer modes in detail. [16]

7. Explain the vector processing in detail with diagram [16]

8. (a) Explain the working of 8 x 8 Omega Switching network.
   (b) Explain system bus structure for multiprocessors with a neat sketch. [8+8]

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