Code No: R22122 **R10** SET - 1

II B. Tech II Semester, Supplementary Examinations, Dec – 2012
COMPUTER ORGANIZATION AND ARCHITECTURE
(Information Technology)

Time: 3 hours Max. Marks: 75

Answer any **FIVE** Questions
All Questions carry **Equal** Marks
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1. a) Explain the concept of Von Neumann Machine.
   b) List various registers in a computer along with their purpose

2. Explain various Addressing modes in 8086

3. a) What are the various kinds of Hazards in Pipelining?
   b) Distinguish between horizontal and vertical instruction format

4. A pipelined processor proceses each instruction in four steps, as follows
   Fetch : Read the instruction from the memory
   Decode: Decode the instruction and fetch the source operands
   Execute: Perform the operation specified by the instruction.
   Write : Store the result in the destination location
   Consider the following sequence of instructions
   ADD #20, R0.R1
   AND #3A, R1,R4
   MUL #3, R4,R3
   ADD #R3, R4,R5.
   Give the pipeline timing diagram to describe the operation being performed by each pipeline stage during each of the clock cycles 1 through 4

5. Explain in detail about Micro instruction execution.

6. Explain about Asynchronous and Synchronous DRAMs

7. What is difference between isolated I/O and memory-mapped I/O? What are advantages and disadvantages?

8. Write the differences between tightly coupled multiprocessors and loosely coupled multiprocessors from the view point of hardware organization and programming techniques.
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Code No: R22122 **R10** SET - 2

II B. Tech II Semester, Supplementary Examinations, Dec – 2012
COMPUTER ORGANIZATION AND ARCHITECTURE
(Information Technology)

Time: 3 hours Max. Marks: 75

Answer any **FIVE** Questions
All Questions carry **Equal** Marks
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1. a) Explain the functioning of a Digital Computer
   b) Discuss Booth's algorithm with illustrations.

2. Explain in detail about register organization of Pentium Processor

3. Explain about RISC architecture.

4. a) Why was microprogramming used on many processors?
   b) Why have modern processors gone away from this technique?
   c) What are the pros and cons of fixed length and variable length instruction encodings?

5. a) Give the typical horizontal and vertical microinstruction formats.
   b) Discuss briefly about Nano-programming

6. Explain briefly about
   a) Demand Paging
   b) Segmentation

7. Give a detailed account of Direct Memory Access(DMA)

8. Explain Cache Coherence in multiprocessor
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Code No: R22122 **R10** SET - 3

II B. Tech II Semester, Supplementary Examinations, Dec – 2012
COMPUTER ORGANIZATION AND ARCHITECTURE
(Information Technology)

Time: 3 hours Max. Marks: 75

Answer any **FIVE** Questions
All Questions carry **Equal** Marks
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1. Explain a Booth's algorithm for 'Multiplication of signed-2's compliment numbers' with a neat flow chart.

2. Explain register transfer process and control function with suitable examples.

3. a) Explain Instruction execution characteristics of RISC processors.
   b) Why does pipelining improve performance?

4. Draw the architecture of 8085 processor and Explain.

5. Explain Micro programming. Discuss the significance of vertical instruction formats for microprogramming.

6. a) Describe a magnetic tape drive and it's controller.
   b) Explain the concept of ROM

7. a) Why does DMA have priority over the CPU when both request a memory transfer? Explain with suitable example?
   b) Discuss the four models data transfer between CPU and I/O devices and compare them

8. Explain in detailed about symmetric multi processors.
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Code No: R22122 **R10** SET - 4

II B. Tech II Semester, Supplementary Examinations, Dec – 2012
COMPUTER ORGANIZATION AND ARCHITECTURE
(Information Technology)

Time: 3 hours Max. Marks: 75

Answer any **FIVE** Questions
All Questions carry **Equal** Marks
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1. Explain a Hardware algorithm for 'Divide' operation with a neat flow chart.

2. Discuss various key design issues of an instruction format.

3. Explain about 8086 processor family

4. Define the following
   a) Micro operation
   b) Micro Instruction
   c) Micro program
   d) Micro code

5. A Computer needs 2K bytes of RAM and 4K bytes of ROM. How many RAM chips and ROM chips are needed if there are only 128x8 RAM chips and 512x8 ROM chips are available?

6. Show the connection model of Memory to the CPU and explain the operation and chip select options?

7. Explain about
   a) Isolated Vs Memory Mapped I/O
   b) I/O Bus Vs Memory Bus.

8. What is cache coherence? Explain different solutions to the cache coherence problem.
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