Code No: V3108 **R07** **Set No: 1**

III B.Tech. I Semester Supplementary Examinations, November/December - 2012

COMPUTER SYSTEM ORGINAZATION

(Electrical and Electronics Engineering)

Time: 3 Hours **Max Marks: 80**

Answer any FIVE Questions

All Questions carry equal marks

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1. a) Represent the number $(+46.5)_{10}$ as a floating –point binary number with 24 bits. The normalized fraction mantissa has 16 bits and the exponent has 8 bits.
   b) Perform the arithmetic operations (+70) + (+80) and (-70)+(-80) with binary numbers in signed 2's complement representation . Use eight bits to accommodate each number together with its sign. Show that overflow occurs in both cases, that the last two carries are unequal, and that there is a sign reversal. [8+8]

2. a). Give list of 16 logical micro operations and explain truth tables for 16 functions in detail.
   b) With the arithmetic circuit function table explain about the operation of 4- bit arithmetic circuit [8+8]

3. a) Describe in detail about input output instructions
   b) Convert the following expressions from infix to reverse Polish notation.
      i. A* B+ C*D +E*F
      ii. A*B+A*(B*D+C*E)
      iii. A+B*[C*D+E*(F+G)]
      iv. $\frac{A+[B+C*9(D+E)]}{F*(G+H)}$ [8+8]

4. A compute has 16 registers, an ALU (arithmetic logic unit) with 32 operations, and a shifter with eight operations, all connected to a common bus system.
   i) Formulate a control word for a micro-operation.
   ii) Specify the number of bits in each field of the control word and give a general encoding scheme.
   iii) Show the bits of the control word that specify the micro-operation R4←R5+R6 [16]

5. a) Describe in detail about segmented paged mapping.
   b) What is the transfer rate of an eight –track magnetic tape whose speed is 120 inches per second and whose density is 1600 bits per inch? [8+8]

6. a) Give the circuit diagram of 4 X 4 FIFO buffer.
   b) Discuss in detail about daisy chaining method of establishing priority in I/O organization. [8+8]

7. a) Explain in detail about the sequence of steps to be performed in instruction pipeline.
   b) Describe in detail about vector processing and give the representative application areas where vector processing is applicable .Also give the instruction format for vector processor. [8+8]

8. a)Describe in detail about hyper cube interconnection and draw the hyper cube structure for n=1,2 and 3
   b) Explain about serial arbitration procedure in detail. [8+8]

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Code No: V3108 **R07** **Set No: 2**

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Time: 3 Hours **Max Marks: 80**

Answer any FIVE Questions

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1. a) Show the bit configuration of a 24 –bit register when its content represents the decimal equivalent of 295:
   i) in binary ii) in BCD iii) in ASCII using eight bits with even parity
   b) Show that the exclusive-OR function x=A⊕B⊕C⊕D is an odd function. Show that x=1 only when the total number of 1's in A, B, C and D is odd. [8+8]

2. a) Consider the following register transfer statements for two 4-bit registers R1 and R2.
   xT: R1←R1+R2
   X'T: R1←R2
   Every time that variable T=1, either the content of R2 is added to the content of R1 if x=1,or the content of R2 is transferred to R1 if x=0.Draw a diagram showing the hardware implementation of the two statements .Use block diagrams for the two 4-bit registers, a 4-bit adder, and a quadruple 2-to 1 line multiplexer that selects the inputs to R1. In the diagram, show how the control variables x and T selects the inputs of the multiplexer and the load input of register R1.
   b) Describe in detail about the memory transfer and explain with operation of memory unit. [8+8]

3. a) What is program interrupt and discuss about the flow chart for the interrupt cycle .
   b) Give block diagram of a 64 word stack and explain briefly about stack organization. [8+8]

4. a) Describe in detail about micro-programmed control organization.
   b) Explain in detail about the block diagram of a control memory and the associated hardware needed for selecting the next micro instruction address. [8+8]

5. a) A magnetic disk system has the following parameters:
   T_s= Average time to position the magnetic head over a track
   R=Rotation speed of disk in revolutions per second
   N_t= Number of bits per track
   $N_{s=}$ Number of bits per sector
   Calculate the average tine T_a that it will take to read one sector.
   b) Describe in detail about the organization of the memory mapping table in a paged system. [8+8]

6. a) Describe in detail about the block diagram of a typical asynchronous communication interface.
   b) Give a detailed note on direct memory access. [8+8]

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7. a) Explain about the flow diagram of four segment CPU pipeline.
   b) Describe in detail about the problems encountered in instruction pipeline and discuss about handling branch instructions. [8+8]

8. a) What is cross bar switch and explain this with block diagram.
   b) Discuss the differences between tightly coupled multiprocessors and loosely coupled multiprocessors from the viewpoint of hardware organization and programming techniques. [8+8]

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Code No: V3108 **R07** **Set No: 3**

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COMPUTER SYSTEM ORGINAZATION

(Electrical and Electronics Engineering)

Time: 3 Hours **Max Marks: 80**

Answer any FIVE Questions

All Questions carry equal marks

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1. a) What is the radix of the numbers if the solution to the quadratic equation x^2-10x +31=0 is x=5 and x=8?
   b) Discuss in detail about error detection codes. [8+8]

2. a) The 8 –bit registers AR,BR,CR and DR initially have the following values:
   AR=11110010
   BR=11111111
   CR-10111001
   DR=11101010
   Determine the 8-bit values in each register after the execution of the following sequence of micro operations.
   AR←AR+BR
   CR← CR ^ DR
   BR←BR+1
   AR←AR-CR
   b) Explain in detail about one stage of logical unit with its functional table. [8+8]

3. a) What is addressing mode and discuss in detail about different addressing modes.
   b) Give the typical program control instructions and also explain about conditional branch instructions in detail. [8+8]

4. a) Show how a 9-bit micro-operation field in a microinstruction can be divided into subfields to specify 46 micro-operations. How many micro-operations can be specified in one micro instruction?
   b) Formulate a mapping procedure that provides eight consecutive micro-instructions for each routine. The operation code has six bits and the control memory has 2048 words. [8+8]

5. a) A computer uses RAM chips of 1024 X 1 capacity.
   (i) How many chips are needed, and how should their address lines be connected to provide a memory capacity of 1024 bytes?
   (ii) How many chips are needed to provide a memory capacity of 16K bytes? Explain in words how the chips are to be connected to the address bus.
   b) Describe in detail about mapping procedures when considering the organization of cache memory. [8+8]

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6. a) What is the difference between isolated I/O and memory mapped I/O ? What are the advantages and disadvantages of each?
   b) Information is inserted into a FIFO buffer at a rate if m bytes per second. The information is deleted at a rate of n byte per second. The maximum capacity of the buffer is k bytes.
   i) How long does it take for an empty buffer to fill up when m>n?
   ii) How long does it take for a full buffer to empty when m<n?
   iii) Is the FIFO buffer needed if m=n? [8+8]

7. a)Explain in detail about 4-segment pipeline with its space time diagram and also give the speed up of a pipeline processing over an equivalent non pipeline processing.
   b) Describe in detail about RISC pipeline. [8+8]

8. a)Give and explain about the solutions for cache coherence problem.
   b) Explain about inter-processor synchronization and describe about mutual exclusion with semaphores. [8+8]

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COMPUTER SYSTEM ORGINAZATION

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1. a) Perform the subtraction with the following unsigned binary numbers by taking the 2's complement of the subtrahend.
   i) 11010-10000 ii) 11010-1101
   iii)100-110000 iv) 1010100-1010100
   b) Compare and contrast multiprocessors and multi-computers. [8+8]

2. a) Explain with functional table about the stage of arithmetic logic shift unit.
   b) What is wrong with the following register transfer statements?
   i) xT: AR←$\overline{AR}$,AR←0 ii) yT: R1←R2,R1←R3 iii) zT: PC← AR, PC←PC+1 [8+8]

3. a) Give the flowchart that summarizes all memory reference instructions.
   b) Describe in detail about the basic characteristics of RISC processor. [8+8]

4. a) Describe in detail about the design of decoding of micro-operation fields .
   b) Explain about mapping from instruction code to microinstruction address in detail. [8+8]

5. a) A computer employs RAM chips of 256 X 8 and ROM chips of 1024 X 8. The computer system needs 2K bytes of RAM, 4K bytes of ROM, and four interface units, each with four registers. A memory –mapped I/O configuration is used. The two highest- order bits of the address bus are assigned 00 for RAM, 01 for ROM and 10 for interface registers.
      i) How many RAM and ROM chips are needed?
      ii) Draw a memory address map for the system.
      iii) Give the address range in hexadecimal for RAM, ROM and interface.
   b) Explain in detail about the organization of associative memory and also give the match logic for one word of associative memory. [8+8]

6. a) How many characters per second can be transmitted over a 1200 –baud line in each of the following modes? (Assume a character code of eight bits.)
      i) Synchronous serial transmission
      ii) Asynchronous serial transmission with two stop bits.
      iii) Asynchronous serial transmission with one stop bit.
   b) Give example of I/O interface unit and with a block diagram. [8+8]

7. a) What is arithmetic pipeline and what are sub-operations performed in arithmetic pipeline? Explain about the pipeline for floating point addition and subtraction.
   b) Elucidate about SIMD array processors in detail. [8+8]

8. a) Delineate about parallel bus arbitration technique.
   b) Construct a diagram for a 4 X 4 omega switching network. Show the switch setting required to connect input 3 to output 1. [8+8]

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