Code: 9A05406
B.Tech II Year II Semester (R09) Regular & Supplementary Examinations, April/May 2013
COMPUTER ORGANIZATION
(Common to ECC and CSE)
Time: 3 hours
Answer any FIVE questions
All questions carry equal marks
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- 1 With the help of a neat diagram explain the interconnection of processor and main memory.
- 2 (a) Explain the operation of 4-bit adder-subtractor with example.
  - (b) Give hardware implementations to perform logic and shift operations.
- 3 Discuss in detail the design of control unit with block diagram.
- 4 (a) Perform the arithmetic operations given below with binary and negative numbers in signed -2's complement representation. Use seven bits to accommodate each number together with its sign. (i) (-53) + (-80) (ii) (-53) (+80)
  - (b) Explain the decimal division algorithm flowchart with a suitable example.
- 5 (a) Explain with the help of a block diagram the cache memory system.
  - (b) A block set-associative cache consists of 64 blocks divided into 4 block sets. The main memory contains 4096 blocks; each consists of 128 words of 16 bits length.
    (i) How many bits are there in main memory?
    - (ii) How many bits are there in each of the TAG, SET and WORD fields?
- 6 (a) How are hardware controlled I/O also known as? Discuss the merits of the same.
  - (b) Discuss in detail interrupt driven I/O.
- 7 (a) Explain the attached array processor with conventional computer.
  - (b) What is structural hazard?
- 8 (a) Explain memory update policies to prevent cache coherence problem.
  - (b) Discuss on the advantages of loosely coupled systems.

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B.Tech II Year II Semester (R09) Regular & Supplementary Examinations, April/May 2013 COMPUTER ORGANIZATION (Common to ECC and CSE)	
Time: 3 hours Max Marks: 70	
Answer any FIVE questions All questions carry equal marks	
1 (a) (b)	Write a note on performance measure. Explain basic operational concepts of a computer with neat diagram.
2 (a) (b)	Explain interrupt cycle with flow chart. Describe general branch and call/return instructions.
3 (a)	Explain mapping techniques to convert an operation to a micro routine address in control memory.
(D)	Explain the operation of a micro programmed control unit.
4 (a) (b)	Multiply 100111 with 11011 using booths algorithm. Give and explain the hardware implementation for signed 2's complement addition and subtraction.
5	Explain the various features and applications of DVD.
6 (a) (b)	Explain the PCI bus commands. Draw and explain the timing diagram for PCI read operation.
7	Classify the pipeline processors and explain them in detail.
8 (a) (b)	What do you mean by bus arbitration? Explain the serial arbitration technique with the help of a neat diagram. State advantages and disadvantages.
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B.Tech II Year II Semester (R09) Regular & Supplementary Examinations, April/May 2013 **COMPUTER ORGANIZATION** (Common to ECC and CSE) Time: 3 hours Max Marks: 70 Answer any FIVE questions All questions carry equal marks Explain in detail on floating-point representation. Support your answer with examples wherever necessary. 2 (a) Explain the setup involved in instruction execution using state diagram. Explain the various addressing modes of an instruction. (b) 3 (a) Write about the control memory in detail. Compare and contrast hardwired control and micro-programmed control. Is it possible (b) to have a hardwired control associated with a control memory? Draw the flow chart for multiplication of two signed magnitude fixed point number and 4 (a) explain with a numerical example. With the help of diagram explain "all serial decimal addition". (b) Explain the concept of cache updating and the need for its updating. Discuss the 5 (a) different updating systems. Explain the necessity of replacement algorithms for cache memory. (b) Explain the arrangement for group handling of priority interrupts. 6 (a) Explain the need for assigning priorities to the interrupts. (b) Explain the two phases instruction fetch and execute.

- 8 (a) Explain with the help of a neat sketch how a time shared bus inter connection system for multiple processors provide a common communication path connecting all of the functional units.
  - Draw the sketch and explain the multiprocessor with unidirectional buses. (b)

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- 4 (a) Explain non restoring method of division with a simple example.
  - (b) With the help of a flow chart explain the division operation.
- 5 Describe and explain in detail optical memories.
- 6 (a) What is I/O interface? Explain I/O interface with the help of a block diagram.
  (b) With the help of a neat sketch explain the I/O interface for I/O device and I/O interface for O/P device.
- 7 (a) Explain the hardware organization for four stage instruction pipeline.
  - (b) What is a data hazard?
- 8 Discuss the cache coherence in the centralized share memory architecture.

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