## Set No. 1

## IV B.Tech II Semester Supplementary Examinations, July/August, 2012 <br> DIGITAL CONTROL SYSTEMS <br> (Electrical and Electronics Engineering)

Time: 3 hours
Max. Marks: 80

## Answer any FIVE Questions <br> All Questions carry equal marks <br> *****

1. a) Explain different methods of $\mathrm{A} / \mathrm{D}$ conversion?
b) Explain the sample and hold circuits with a neat circuit diagram.
2. a) Obtain the inverse $z$-transform of the following:
(i) $X(Z)=[Z(Z+2)] /\left[(Z-1)^{2}\right]$
(ii) $X(Z)=\left[Z^{-2}\right] /\left[\left(1-Z^{-1}\right)^{3}\right]$
b) Obtain the $Z$-transform of the following
(i) $X(S)=\frac{a}{s^{2}(s+a)}$
(ii) $X(S)=\frac{s}{\left(s^{2}-\omega^{2}\right)}$
3. a) Explain bounded-input, bounded-output stability.
b) Solve the following difference equation by the use of Z-transform method.
$X(K+2)+3 X(K+1)+2 X(K)=0 ;$ with $X(0)=0, X(1)=1$
4. Consider the discrete control system represented by the transfer function. $G(Z)=\frac{Z^{-1}\left(1+Z^{-1}\right)}{\left(1+0.5 Z^{-1}\right)\left(1-0.5 Z^{-1}\right)}$ Obtain the state space representation in the diagonal form. Also, find its state transition matrix.
5. a) State and explain the Obsevability theorem.
b) Derive the relation between controllability, obeservabilit and transfer function.
6. a) Determine the Z -transform of the following sequence:

$$
f(K)=\left\{\begin{array}{l}
1, K=0, \text { and }, \text { even }, \text { int eger } \\
-1, K=\text { odd }, \text { int eger }
\end{array}\right.
$$

b) State Z- Transform and obtain the relation between Z-plane and S-plane transformations.

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7. a) Write short notes on PID controllers
b) Explain the design procedure of lead-lag compensator in W-plane.
8. Explain the reduced order state observer with block diagram.

## Set No. 2

## IV B.Tech II Semester Supplementary Examinations, July/August, 2012 DIGITAL CONTROL SYSTEMS <br> (Electrical and Electronics Engineering)

Time: $\mathbf{3}$ hours

Max. Marks: 80

## Answer any FIVE Questions <br> All Questions carry equal marks <br> *****

1. What are the advantages and disadvantages of digital control system over analog control system? With suitable diagram explain any two methods of digital to analog conversion.
2. a)Find the Z-Transform of the following
(i) $F(S)=\frac{1}{s^{2}(s+1)}$ (ii) $f(t)=t \sin (\omega t)$
b) State and prove "initial and final "values theorems.
3. a) Explain the mapping between S-plain and Z-plain.
b) Solve the following difference equation $X(K)-0.6 X(K-1)-0.812 X(K-2)+0.67 X(K-3)-0.12 X(K-4)=Y(K)$
All the initial conditions are assumed to be zero.
4. A discrete system is described by the difference equation

$$
\begin{aligned}
& Y(K+2)+3 Y(K+1)+2 Y(K)=r(K) \\
& Y(0)=Y(1)=0, T=1 \text { Sec. }
\end{aligned}
$$

a) Determine a state variable model for the system. Draw the state diagram.
b) Find the state transition matrix
5. Examine whether the discrete data system given below.
$X(K+1)=\left[\begin{array}{cc}0 & 1 \\ -3 & -4\end{array}\right] X(K)+\left[\begin{array}{c}1 \\ -1\end{array}\right] u(K)$
$Y(K)=\left[\begin{array}{ll}1 & 0\end{array}\right] X(K)$
Is (i) State controllable (ii) Output controllable (iii) Observable
6. a) Solve the following difference equation by the use of Z-transform method $X(K+2)+3 X(K+1)+2 X(K)=0$; with $X(0)=X(1)=1$.
b)Explain the mapping between S-plane and Z-plane

## Set No. 2

7. The digital control process of a unity feedback system is described by the transfer function $G_{h o} G_{p}(Z)=\frac{K(Z+0.5)}{(Z-1)(Z-0.5)}$,
Design a cascade phase -lag controller with the transfer function $D(Z)=K_{c} \frac{Z-Z_{1}}{Z-P_{1}}$, so that the following design specifications are satisfied.
(i) $K_{V}=6$
(ii) The dominant roots of the closed loop characteristic equation are approximately at $Y(K)$
(iii) The maximum overshoot is $\leq 15$ present.
8. Consider the digital process with the state equation described by
$X(K+1)=\left[\begin{array}{cc}0 & 1 \\ -1 & 1\end{array}\right] X(K)+\left[\begin{array}{l}0 \\ 1\end{array}\right] U(K)$ and $Y(K)=\left[\begin{array}{ll}2 & 0\end{array}\right] X(K)$
Design a full order observer which will observe the states $X_{1}(K)$ and $X_{2}(K)$
from the output $Y(K)$, having dead beat response.

## Set No. 3

## IV B.Tech II Semester Supplementary Examinations, July/August, 2012 DIGITAL CONTROL SYSTEMS (Electrical and Electronics Engineering)

Time: 3 hours
Max. Marks: 80

## Answer any FIVE Questions All Questions carry equal marks

1. a) Explain the functions of the following in a digital control system:
(i) Hold circuit (ii) sampling (iii) Data hold
b) Describe the following parameters
(i) Acquisition time (ii) Aperture time and (iii) settling time
2. a) Find the inverse Z-transform of the following
(i) $X(Z)=Z(Z+2) /(Z-1)^{2}$ (ii) $\left(2 Z^{3}+Z\right) /(Z-2)^{2}(Z-1)$
b) Explain the procedure for obtaining pulse transfer function of a closed loop transfer function.
3. a) Determine the pulse transfer function of two cascaded system, each described by the difference equation. $Y(K)=0.5 Y(K-1)+r(K)$
b) Explain bounded-input, bounded-output stability
4. A discrete - time system is described by the difference equation.
$Y(K+2)+5 Y(K+1)+6 Y(K)=u(K)$
$Y(0)=Y(1)=0 ; T=1$ Sec.
Determine a state model in canonical form.
a) Find the state transition matrix
b) For input $u(K)=1$, for $K \geq 0$, Find, $Y(K)$.
5. Investigate the controllability and observability of the following system.
$\left[\begin{array}{l}X_{1}(K+1) \\ X_{2}(K+1)\end{array}\right]=\left[\begin{array}{ll}1 & -2 \\ 1 & -1\end{array}\right]\left[\begin{array}{l}X_{1}(K) \\ X_{2}(K)\end{array}\right]+\left[\begin{array}{cc}1 & -1 \\ 0 & 0\end{array}\right] u(K)$
$\left[\begin{array}{l}Y(K) \\ X(K)\end{array}\right]=\left[\begin{array}{ll}1 & 0 \\ 0 & 1\end{array}\right]\left[\begin{array}{l}X_{1}(K) \\ X_{2}(K)\end{array}\right]$

## Set No. 3

6. a) Explain the mapping between S-plane and Z-plane.
b) Using Jury's stability criterion, find the range of K for which the characteristic equation given below,
$Z^{3}+K Z^{2}+1.5 Z-(K+1)=0$ is representing the closed loop stable system.
7. a) Explain the design procedure in the $\omega$-plane of lag compensator.
b) Explain the design of digital control through deadbeat response method.
8. Draw the schematic diagram of full order observer. State the salient steps involved in design of state feedback controller through pole placement.

## Set No. 4

## IV B.Tech II Semester Supplementary Examinations, July/August, 2012 <br> DIGITAL CONTROL SYSTEMS <br> (Electrical and Electronics Engineering)

Time: 3 hours
Max. Marks: 80

## Answer any FIVE Questions <br> All Questions carry equal marks <br> *****

1. a) With a suitable circuit, explain the operation of sampler and hold devices.

Also derive the transfer function of zero-order hold.
b) With help of diagram explain the successive approximation analog to digital converter.
2. a)Obtain the Z -transform of
(i) $\quad f(t)=t^{2}$ (ii) $f(t)=e^{(-a t)} \sin \omega t$
b) Explain the different properties and theorems of Z-transforms.
3. For the sampled data system shown in fig., find the response to unit step input if

$$
G(s)=\frac{1}{s+1}
$$


4. a) Using Z-transform method find the state transition matrix for the digital system is given by. $X(K+1)=\left[\begin{array}{cc}0 & 1 \\ -3 & -4\end{array}\right] X(K)$
b) Explain the properties of state transition matrix.
5. a) Derive the necessary condition for digital control system
$X(K+1)=G X(K)=H u(K)$
$Y(K)=C X(K)$ to be output controllable and observable.
(b) $Y(K)=\left[\begin{array}{ll}1 & 0 \\ 0 & 1\end{array}\right] X(K)$

Is (i) output controllable (ii) Observable.

## Set No. 4

6. a) State and explain Jury stability test applied to discrete time controls. Consider the digital system shown in figure.
b) Find the range of K for the system to be stable using Jury stability test.

7. A block diagram of a digital control system is shown in Figure. Design a PID controller $\mathrm{D}(\mathrm{Z})$, to eliminate the steady state error due to a step input and simultaneously realizing a good transient response, and the ramp error constant Kv should be equal 5 .

8. Consider the digital process with the state equation described by
$X(K+1)=\left[\begin{array}{cc}1 & -1 \\ -1 & 0\end{array}\right] X(K)+\left[\begin{array}{l}1 \\ 0\end{array}\right] U(K)$ and $Y(K)=\left[\begin{array}{ll}0 & 2\end{array}\right] X(K)$
Design a full order and reduced order observer which will observe the states $X_{1}(K)$ and $X_{2}(K)$ from the output $Y(K)$, having dead beat response.
