

Code No: R31042

R10

Set No: 1

III B.Tech. I Semester Supplementary Examinations, May - 2013

DIGITAL IC APPLICATIONS

(Common to Electronics and Communications Engineering & Electronics and Instrumentation Engineering & Bio-Medical Engineering & Electronics and Computer Engineering)

Time: 3 Hours

Max Marks: 75

Answer any FIVE Questions
All Questions carry equal marks

1. With a suitable diagram explain about CMOS AND-OR inverter gate.
2. Using karnaugh map, find a minimal sum of products expression for each of the following logic functions.
i) $\sum_{m,m\bar{m}}(1,3,5,6,7)$ ii) $\sum_{m,m\bar{m}}(1,4,5,6,7,9,14,15)$
3. Explain about 2 input LS -TTL NAND gate.
4. Write about look ahead carry generator.
5. Explain the following
 - i) Define flip flop.
 - ii) Explain how to build a J-K flip flop using a T-flip flop with enable and combinational logic?
6. Define PLD? With neat diagram explain about PLD.
7. Draw a logic symbol for and determine the size of a ROM that realizes a combinational logic function that can perform the function either a 74X381 OR a 74x382 depending on the value of a single mode input.
8. (a) Write the differences between static and dynamic RAM'S.
(b) Explain about internal structure and timing of DRAM'S.



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Time: 3 Hours**Max Marks: 75**

Answer any FIVE Questions
All Questions carry equal marks

1. Write a neat diagram explain about 3-input CMOS NOR gate .
2. Using karnaugh map, find a minimal sum of products expression for each of the following logic functions.
i) $f = \prod_{WXYZ}(1,4,5,6,7)$ ii) $f = \sum_{WXYZ}(0,1,6,7,8,9,14,15)$.
3. Explain about TTL logic levels and noise margins.
4. Discuss about BINARY ADDER-SUBTRACTOR.
5. Draw karnaugh maps and derive excitation equations for S-R latch with enable.
6. (a) Define programmable logic array.
(b) With neat diagram explain about programmable logic arrays.
7. Explain how to design a 2MX8 SRAM using HM628512 SRAMS and a combinational MSI part as building blocks?
8. a) Define ROM?
b) Discuss about various commercial ROM types, timings and applications.



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Time: 3 Hours

Max Marks: 75

Answer any FIVE Questions
All Questions carry equal marks

1. (a) Define i) fan-in ii) fan-out iii) power dissipation iv) propagation delay.
(b) Explain "LATCH-UP" and the circumstances under which it occurs.
2. Prove Shannon's expansion theorems.
3. Explain about basic ECL inverter circuit.
4. a) Define cascading comparators.
b) Write about design considerations of cascading comparators
5. Show that a 4-bit one's complement adder with end around carry is a feedback sequential circuit.
6. (a) Define i) PROM ii) PLA iii) PAL
(b) Discuss about the comparison of PROM, PLA, and PAL
7. Draw the logic symbol for and determine the size of a ROM that realizes an 8x8 combinational multiplier.
8. (a) Define ROM.
(b) Discuss about various commercial ROM types, timings and applications



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Time: 3 Hours

Max Marks: 75

Answer any FIVE Questions
All Questions carry equal marks

1. (a) Explain why the number of CMOS inputs connected to the output of a CMOS gate generally is not limited by DC fanout considerations.
(b) Discuss the advantages and disadvantages of larger versus pull-up resistor for open drain CMOS outputs.
2. (a) Show that an n-input OR gate can be replaced by (n-1) 2-input OR gates .
(b) Justify whether the above statement can be made for NOR gates.
3. Write about CMOS/TTL interfacing.
4. (a) Define combinational multiplier.
(b) Write about the design considerations of a combinational multiplier.
5. Explain the synchronous design methodology in case of sequential circuit.
6. (a) Define PLD?
(b) With neat diagram explain about PLD
7. Draw logic symbol for and determine the size of a ROM that realize an 8x8 combinational multiplier.
8. (a) Differentiate between STATIC and DYNAMIC RAMS .
(b) Explain the internal structure and timing of DRAM'S.

