Code No: V3121 **R07** **Set No: 1**

III B.Tech. I Semester Supplementary Examinations, April/May - 2013

DIGITAL IC APPLICATIONS

(Common to ECE, EIE)

Time: 3 Hours **Max Marks: 80**

Answer any FIVE Questions

All Questions carry equal marks

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1. a) Explain the effect of transition time on speed of a CMOS device. Use equivalent circuits for analyzing transition times of a CMOS inverter output using models of a CMOS HIGH-to-LOW transition and also for LOW-to-HIGH transition.
   b) Explain the operation of a basic CMOS inverter using switch model and also explain its logical operation. [12M+4M]

2. a) Explain the operation of a basic ECL OR/NOR gate using circuit diagram and function table.
   b) Describe the key benefits of Schottky transistors in TTL.
   c) Using the maximum allowable resistor values calculate and write which resistor dissipates more power, the pull-down for an unused LS-TTL NOR-gate input, or the pull-up for an unused LS-TTL NAND gate input? [8M+3M+5M]

3. Explain in detail the steps in HDL based design flow using a block diagram. [16M]

4. a) Write the syntax of the following
   (i) VHDL component statement.
   (ii)VHDL component declaration.
   (iii)VHDL generic declaration with an entity declaration.
   b) Explain dataflow design. [6M+10M]

5. a) Explain the functioning of a 74x138 3-to-8 decoder using its logic diagram and truth table.
   b) Design a 5-to-32 decoder using 74x138s. [9M+7M]

6. a) Write a VHDL program for implementing a floating point encoder.
   b) Write a VHDL program for implementing a dual parity encoder. [8M+8M]

7. a) Explain in detail clock-skew as an impediment to synchronous design.
   b) Implement a 4-bit ring counter using 74x194 and explain the operation using relevant timing diagram and state diagram. [8M+8M]

8. a) With the help of timing diagrams explain the read and write operations of SRAM.
   b) Explain the internal structure of synchronous SRAM. [10M+6M]

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Code No: V3121 **R07** **Set No: 2**

III B.Tech. I Semester Supplementary Examinations, April/May - 2013

DIGITAL IC APPLICATIONS

(Common to ECE, EIE)

Time: 3 Hours **Max Marks: 80**

Answer any FIVE Questions

All Questions carry equal marks

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1. a) Explain the effect of propagation delays on a CMOS device. Use propagation delay wave forms ignoring rise time, fall time and t_pHL, t_pLH measured at midpoints of transitions.
   b) Which would you expect to have a bigger effect on the power consumption of a CMOS circuit, a 5% increase in power-supply voltage or a 5% increase in internal and load capacitance?
   c) Explain the operation of a CMOS 2 input NAND gate using switch model. [7M+4M+5M]

2. a) Explain the operation of a 2 input LS-TTL NAND gate using circuit diagram and function table.
   b) Present the details of TTL logic levels, TTL noise margins and TTL fan-out. [8M+8M]

3. a) Explain the terms VHDL entity and VHDL architecture. Also explain the wrapper concept and hierarchical use of VHDL entities and architectures.
   b) Write VHDL function for converting INTEGER in to STD_LOGIC_VECTOR.
   c) Classify data types and explain. [6M+6M+4M]

4. a) Write VHDL entity and architecture for an arbitrary-width bus inverter.
   b) Write the syntax of a VHDL if statement.
   c) Explain simulation. [6M+4M+6M]

5. a) Explain the functioning of a 74x151 8-input, 1-bit multiplexer using logic diagram and truth table.
   b) Design a 32-to-1 multiplexer using 74x151 Ics. [8M+8M]

6. a) Write a VHDL program for implementing a 16-bit barrel shifter.
   b) Write a VHDL program for implementing a floating point encoder. [8M+8M]

7. a) Explain in detail gating the clock with reference to impediments to synchronous design.
   b) Implement a 4-bit 8-state Johnson counter using 74x194 and explain the operation using relevant timing diagram. [8M+8M]

8. a) Explain the internal ROM structure of a simple 8x4 diode ROM. Explain 2-D decoding using internal structure of any relevant ROM.
   b) Draw the internal structure of ROM showing use of control inputs and explain timing diagram in detail. [8M+8M]

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Code No: V3121 **R07** **Set No: 3**

III B.Tech. I Semester Supplementary Examinations, April/May - 2013

DIGITAL IC APPLICATIONS

(Common to ECE, EIE)

Time: 3 Hours **Max Marks: 80**

Answer any FIVE Questions

All Questions carry equal marks

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1. a) Discuss the pros and cons of larger vs. smaller pull-up resistors for open drain CMOS outputs.
   b) Describe the circuit behavior of a CMOS inverter with resistive load for both CMOS LOW and HIGH outputs. Use necessary equivalent circuits.
   c) Explain why the number of CMOS inputs connected to the output of a CMOS gate generally is not limited by DC fan-out considerations. [4M+9M+3M]

2. a) Explain the operation of a basic ECL inverter /buffer circuit for different inputs.
   b) Explain the concept of logic levels and noise margins with reference to TTL families. [8M+8M]

3. a) Explain the following using examples
   (i) Reserved words (ii) Identifiers (iii) Ports
   b) Write the syntax of VHDL array declarations and examples of VHDL array declarations.
   c) Write VHDL function for converting STD_LOGIC_VECTOR in to INTEGER. [6M+4M+6M]

4. a) Write VHDL entity and architecture for an 8-bit inverter.
   b) Write the syntax of
   (i) Basic VHDL loop statement. (ii) Case statement. (iii) Process statement.
   c) Present the prime-detector architecture using a case statement. [6M+6M+4M]

5. a) Describe the generative structure of an iterative combinational circuit and explain the operation of a iterative comparator circuit.
   b) Explain the characteristics and features of three state buffers using an example and timing diagram. [8M+8M]

6. a) Write a VHDL program for implementing a floating point encoder.
   b) Write a VHDL program for implementing a dual parity encoder. [8M+8M]

7. a) Describe the synchronous system structure using a block schematic and explain the operation using a timing diagram.
   b) Implement a 4-bit ring counter using 74x194 and explain the operation using relevant timing diagram and state diagram. [8M+8M]

8. Draw the basic cell structures of dynamic RAM, internal structure of SDRAM and explain. What is the requirement of refresh cycle? Explain read, burst-write timing diagrams. [16M]

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Code No: V3121 **R07** **Set No: 4**

III B.Tech. I Semester Supplementary Examinations, April/May - 2013

DIGITAL IC APPLICATIONS

(Common to ECE, EIE)

Time: 3 Hours **Max Marks: 80**

Answer any FIVE Questions

All Questions carry equal marks

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1. a) Draw the typical output transfer characteristic of a CMOS inverter and explain the concept of logic levels and noise margins for any typical logic family.
   b) Explain Latch-up and the circumstances under which it occurs?
   c) Consider the dynamic behavior of CMOS output driving a given capacitance of the load. If the load resistance of the charging path is double the resistance of the discharging path, is the rise time exactly twice the rise time? If not, what other factors affect the transition times? [8M+4M+4M]
2. a) Explain diode in detail and explain the operation of diode AND gate using necessary circuits, function table and truth table.
   b) Compare different logic levels of 5-V TTL, 3.3-V TTL and 2.5-V CMOS families and also explain why some inputs are 5-V tolerant and others are not using relevant input structures. [8M+8M]
3. a) Write the syntax of a VHDL entity declaration and architecture definition.
   b) Write about mode with reference to an entity declaration.
   c) Write VHDL program for inhibit function.
   d) Write the syntax of a VHDL package definition. [4M+4M+4M+4M]
4. Explain structural design and write a structural VHDL program for prime number detector. [16M]
5. a) Explain the functioning of a 74x148 8-input priority encoder using a truth table.
   b) Design a 32 input encoder using 74x148 Ics. [8M+8M]
6. a) Write a VHDL program for implementing a 16-bit barrel shifter.
   b) Write a VHDL program for implementing a floating point encoder. [8M+8M]
7. a) Explain in detail asynchronous inputs with reference to impediments to synchronous design.
   b) Implement a 4-bit 8-state Johnson counter using 74x194 and explain the operation using relevant timing diagram. [8M+8M]
8. a) Explain the operation of synchronous SRAM with the help of its internal structure. Also discuss the timing behavior for late-write SSRAM with flow through outputs.
   b) Discuss applications of ROM. [10M+6M]

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