Code No: V3121 **R07** **Set No: 1**

III B.Tech. I Semester Supplementary Examinations, November/December - 2012

DIGITAL IC APPLICATIONS

(Comm. to Electronics and Communications Engineering & Electronics and Instrumentation Engineering)

Time: 3 Hours **Max Marks: 80**

Answer any FIVE Questions

All Questions carry equal marks

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1. (a) Explain the working of a four input CMOS AND-OR-INVERT gate with the help of a circuit diagram and function table. Also draw the logic diagram for it.
   (b) Explain Latch-up and the circumstances under which it occurs?
   (c) Consider the dynamic behavior of CMOS output driving a given capacitance of the load. If the load resistance of the charging path is double the resistance of the discharging path, is the rise time exactly twice the rise time? If not, what other factors affect the transition times? (8+4+4)

2. (a) Explain the operation of a basic ECL inverter /buffer circuit for different inputs.
   (b) What are the factors that have led the IC industry to move toward low power supply voltages in CMOS devices and explain why some outputs are 5-V tolerant and others are not? (8+8)

3. Explain various modeling styles in VHDL with examples. (16)

4. (a) Classify the operators in VHDL and explain with examples.
   (b) Explain access types data types in VHDL with example. (12+4)

5. (a) Explain all the possible designs of subtractor using adders.
   (b) Write a VHDL program for adding and subtracting 8-bit integers of various types. (8+8)

6. Design a 24-bit comparator using three 74x682s, additional gates as required which should compare two 24-bit unsigned numbers P, Q and produce two output bits that indicate whether P=Q or P>Q. Write VHDL code to implement the same. (16)

7. (a) Show how to build a D flip-flop using a T flip-flop with enable and combinational logic.
   (b) Write a VHDL program for a clocked synchronous state machine which has two inputs X, Y and output Z. The output should be 1 if the number of 1inputs on X and Y is a multiple of 4 since reset, and 0 otherwise. (8+8)

8. (a) Explain the operation of synchronous SRAM with the help of its internal structure. Also discuss the timing behavior for late-write SSRAM with flow through outputs.
   (b) Discuss applications of ROM. (10+6)

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Code No: V3121 **R07** **Set No: 2**

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Time: 3 Hours **Max Marks: 80**

Answer any FIVE Questions

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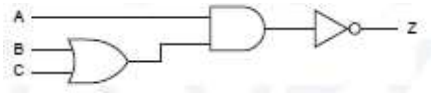
1. (a) Explain the working of a two input CMOS NAND gate with the help of a circuit diagram and function table. Use switch model to explain the operation.
   (b) Explain why the number of CMOS inputs connected to the output of a CMOS gate generally is not limited by DC fan-out considerations.
   (c) Design a CMOS circuit that has functional behavior shown in figure below.



(4+4+8)

2. (a) Explain the several factors to be considered for CMOS/TTL interfacing?
   (b) Compare different logic levels of 5-V TTL, 3.3-V TTL and 2.5-V CMOS families and also explain why some inputs are 5-V tolerant and others are not using relevant input structures. (8+8)

3. (a) Explain the different ways to specify a time delay in a VHDL code using examples.
   (b) Explain the syntax and function of CASE statement. Explain using an example. (10+6)

4. Classify the possible data types that can exist in VHDL and explain each one with example. (16)

5. Design a 16 input priority encoder using two 74x148 encoders and also write a VHDL code to implement it. (16)

6. Explain the general structure of an iterative combinational circuit. Explain the logical operation of a iterative comparator using an algorithm and relevant circuits. Write a VHDL program for 16-bit iterative comparator circuit. (16)

7. (a) Show how to build a J-K flip-flop using a T flip-flop with enable and combinational logic.
   (b) Write a VHDL program for a clocked synchronous state machine with one input, X and one output, UNL. The UNL output should be 1 if and only if X is 0 and the sequence of inputs received on X at the preceding seven clock ticks was 0110111. (8+8)

8. Draw the basic cell structures of dynamic RAM, internal structure of SDRAM and explain. What is the requirement of refresh cycle? Explain read, write, burst-read, burst-write timing diagrams. (16)

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Code No: V3121 **R07** **Set No: 3**

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DIGITAL IC APPLICATIONS

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Time: 3 Hours **Max Marks: 80**

Answer any FIVE Questions

All Questions carry equal marks

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1. (a) Explain the working of a four input CMOS OR-AND-INVERT gate with the help of a circuit diagram and function table. Also draw the logic diagram for it.
   (b) Which would you expect to have a bigger effect on the power consumption of a CMOS circuit, a 5% increase in power-supply voltage or a 5% increase in internal and load capacitance.
   (c) Discuss the pros and cons of larger vs. smaller pull-up resistors for open drain CMOS outputs. (8+4+4)

2. (a) Explain the operation of a 2 input LS-TTL NAND gate using circuit diagram and function table.
   (b) Present the details of TTL logic levels, TTL noise margins and TTL fan-out. (8+8)

3. Write the classification of VHDL statements and explain each one of them. (16)

4. (a) Present the design flow of VHDL and explain each step in detail.
   (b) Explain package declaration and package body using an example. (10+6)

5. Design a combinational circuit to detect a prime number of a 8-bit input and also write a VHDL code to implement it. (16)

6. (a) Write a VHDL program for implementing a floating-point encoder.
   (b) Write a VHDL program for implementing a dual priority encoder. (8+8)

7. (a) Show how to build a T flip-flop using a D flip-flop with enable and combinational logic.
   (b) Design a clocked synchronous state machine with two inputs A, B one output Z that is 1 if
   - A had the same value at each of the two previous clock ticks or
   - B has 1 since the last time that the first condition was true.

   Otherwise the output should be zero. (8+8)

8. (a) Explain the internal ROM structure of a simple 8x4 diode ROM. Explain 2-D decoding using internal structure of any relevant ROM.
   (b) Draw the internal structure of ROM showing use of control inputs and explain timing diagram in detail. (8+8)

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Code No: V3121 **R07** **Set No: 4**

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Time: 3 Hours **Max Marks: 80**

Answer any FIVE Questions

All Questions carry equal marks

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1. (a) Explain the working of a two input CMOS NOR gate with the help of a circuit diagram and function table. Use switch model to explain the operation.
   (b) Under what circumstances is it safe to allow an unused CMOS input to float?
   (c) Design a CMOS circuit that has functional behavior represented by (A′+BC)′ . (4+4+8)

2. (a) Explain the operation of a basic ECL OR/NOR gate using circuit diagram and function table.
   (b) Describe the key benefits of Schottky transistors in TTL.
   (c) Using the maximum allowable resistor values calculate and write which resistor dissipates more power, the pull-down for an unused LS-TTL NOR-gate input, or the pull-up for an unused LS-TTL NAND gate input? (8+3+5)

3. (a) Explain PROCESS statement in VHDL using an example.
   (b) Explain how variable is different than signal in VHDL
   (c) Write the differences between functional simulation and timing simulation. (6+6+4)

4. (a) Explain the program structure of VHDL using a block diagram.
   (b) What are the uses of system, user and work libraries? (10+6)

5. (a) Write a VHDL program for Hamming error correction.
   (b) Explain the operation using logic diagram and truth table of 74x157 2-input 4-bit multiplexer (8+8)

6. (a) Write a VHDL program for comparing 8-bit integers of various types.
   (b) Write a VHDL program for implementing a barrel shifter. (8+8)

7. (a) Show how to build a T flip-flop using a J-K flip-flop with enable and combinational logic.
   (b) Write a VHDL program for a clocked synchronous state machine with one input, X and one output, UNL. The UNL output should be 1 if and only if X is 1 and the sequence of inputs received on X at the preceding seven clock ticks was 0010010. (8+8)

8. (a) With the help of timing diagrams explain the read and write operations of SRAM.
   (b) Explain the internal structure of synchronous SRAM. (10+6)

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