Code No: R21054 **R10** SET - 1

II B. Tech I Semester, Supplementary Examinations, May – 2013
DIGITAL LOGIC DESIGN
(Com. to CSE, IT)

Time: 3 hours Max. Marks: 75

Answer any **FIVE** Questions
All Questions carry **Equal** Marks
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1. a) Subtract 547_{10} from 792_{10} using the excess-3 subtractor.
   b) Encode the decimal numbers using 6,3,1,-1 weighted code. Is it a self-complementing code? (7M+8M)
2. a) Show that the dual of the exclusive-or is equal to its complement
   b) Express the complement of the following function in sum of minterms form
   i) F(x,y,z) = xy+xz ii) F(A,B,C)= π(2,4,5,7) (7M+8M)
3. a) Design a logic circuit having three inputs A,B,C such that output is 1 when A=0 or whenever B=C=1.Also obtain logic circuit using NAND gates.
   b) Simplify the following Boolean function by using the Karnaugh- map method
   F=Σ (0,1,2,8,10,11,14,15) (7M+8M)
4. a) With the help of logic diagram explain a parallel adder/ subtractor using 2's compliment system.
   b) Design a full adder using AND, OR, NOT gates (9M+6M)
5. a) A combinational logic circuit is defined by the flowing Boolean functions
   F_1 = (ABC)' + AC F_2 = A(BC)'+A'B F_3 = A'C+AB Design the circuit with the decoder and external gates.
   b) Draw the logic diagram of 8 to 3 line encoder using three 4 input NAND gates. (8M+7M)
6. a) Realize F=∑m(0,2,3,7,9,11,15,16) using PAL,PLA
   b) List the PLA programming table for the BCD to excess -3 code converter (8M+7M)
7. a) Realize a master slave JK flip-flop using NAND gates and explain its operation and point out how the race around condition is avoided.
   b) Distinguish between sequential system and combinational system (11M+4M)
8. a) Draw the circuit diagram of 4bit ring counter using T-flip-flops and draw the corresponding timing diagrams.
   b) Explain the circuit diagram of 4bit universal shift register? (8M+7M)
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Code No: R21054 **R10** SET - 2

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DIGITAL LOGIC DESIGN
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Time: 3 hours Max. Marks: 75

Answer any **FIVE** Questions
All Questions carry **Equal** Marks
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1. Convert the following numbers
   i) $(1776)_{10}$ to base 6 ii) $(198)_{12}$ to base 10 iii) $(1011011.101)_2$ to base 8
   iv) $(4ACF)_{16}$ to base 12 v) $(1110010.101)_2$ to base 16 (3M+3M+3M+3M+3M)

2. a) Simplify the following Boolean expressions to a minimum number of literals.
   i) (A+B) (A+C')+A'B'+A'C' ii) (B+BC) (B+B'C)(B+D)
   b) Convert the following expression into sum of products and products of sums.
   i) (XY+Z) (Y+Z W) ii) A' + A(A+B') (B+C') (7M+8M)

3. Obtain the simplified expressions in sum of products for the following Boolean functions using Karnaugh-Map.
   i) F(A,B,C,D)=Σ(7,13,14,15) ii) F(w,x,y,z) = Σ (2,3,12,13,14,15)
   iii) F(A,B,C,D) = Σ(0,1,4,7,9,12,14) (5M+5M+5M)

4. a) Implement a full subtractor with two half subtractors and an OR gate.
   b) Write short notes on carry look-ahead adder. (9M+6M)

5. a) Design 8 X 1 multiplexer using 2 X 1 multiplexer
   b) Explain the operation of priority encoder with a neat diagram. (8M+7M)

6. Realize the given functions using a PLA with 6 inputs, 4 outputs and 10 NAND gates:
   i) $F_1(A,B,C,D,E,F) = \sum m(0,1,2,3,7,8,9,10,11,15,32,33,34,35,39,40,41,42,43,45,47)$
   ii) $F_2(A,B,C,D,E,F) = \sum m(8,9,10,11,12,14,21,25,27,40,41,42,43,44,46,57,59)$ (15M)

7. a) Draw the schematic circuit of SR flip-flops with negative edge triggering and explain the operation with the help of truth table.
   b) What are the applications of flip-flops? (12M+3M)

8. a) Design a mod-12counter using SR flip-flops
   b) Explain synchronous and ripple counters compare their merits and demerits. (8M+7M)
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Code No: R21054 **R10** SET - 3

II B. Tech I Semester, Supplementary Examinations, May – 2013
DIGITAL LOGIC DESIGN
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Time: 3 hours Max. Marks: 75

Answer any **FIVE** Questions
All Questions carry **Equal** Marks
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1. a) Find the 9's and 10's complement of the following decimal numbers.
   i) 65,485,963 ii) 46,835,200 iii) 50,000,000
   b) Convert the following decimal numbers to BCD, excess-3 and 6311code
   i) 6593 ii) 4275 iii) 6850 (6M+9M)

2. a) Reduce the following Boolean Expressions
   i) AB+A(B+C)+B'(B+D) ii) A+B+A'B'C
   iii) A'B + A'BC' + A'BCD + A'BC'D'E iv) ABEF + AB(EF)' + (AB)'EF
   b) Obtain the dual and complement of the following functions
   i) A'B+A'BC'+A'BCD+A'BC'D'E ii) ABE F+ABEF'+A'B'EF (8M+7M)

3. Obtain minimal SOP expression for the given Boolean function, using K-map:
   F (A,B,C,D)=Σ(0,1,4,6,8,9,10,12) + d(3,7,11,13,14,15) and draw the circuit using 2-input NAND gates. (15M)

4. a) Design a full adder using half adder and look ahead adders.
   b) Write short notes on ripple adder and subtractor (8M+7M)

5. a) A combinational logic circuit is defined by the flowing Boolean functions
   F_1 = AB+A'B'C' F_2 = A+B+C F_3 = A'B+AB'
   Design the circuit with the decoder and external gates.
   b) Draw the logic diagram of 3 to 8 line decoder with NOR gates. (8M+7M)

6. Implement the following function using
   a) PAL b) PLA
   $F_1(a,b,c,d)=\sum$ m(0,1,2,3,6,9,11)
   $F_2(a,b,c,d)=\sum$m(0,1,6,8,9) (7M+8M)

7. a) Distinguish between flip-flop and latch what is race around conditions how do you eliminate it?
   b) Explain the operation and excitation table of RS-flip-flop with a neat diagram. (7M+8M)

8. a) Draw the circuit diagram of Johnson counter using D-flip-flops and explain its operation with the help of bit pattern.
   b) Compare the merits and demerit of ripple and synchronous counters (10M+5M)
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Code No: R21054 **R10** SET - 4

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DIGITAL LOGIC DESIGN
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Time: 3 hours Max. Marks: 75

Answer any **FIVE** Questions
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1. a) Convert the following
   i) $(564)_{10}$ to excess -3 code ii) $(56.25)_{10}$ to BCD code
   iii) $(101011)_2$ to gray code iv) $(110101)_G$ to binary code.
   b) Convert the decimal number 635.5 to base 7, 8 and 12 (8M+7M)

2. a) Express the following function in sum of min terms and product of max terms.
   i) F (A, B, C) = AB+AB'+B'C ii) F (A, B, C) = (AB+C)(B+AC)
   b) Implement the function Y = AB+A(B+C)+B(B+C) using Boolean theorems. (8M+7M)

3. a) Minimize the following expression using K-map
   i) F (x,y,z,w) = Σm(1,4,7,10,13) + Σd(5,14,15)
   ii) F(A,B,C,D) =Σm(1,3,7,11,15)+Σd(0,2,5)
   b) Use the tabular procedure to simplify the given expression
   F(A,B,C,D) = Σm (0,4,12,16,19,24,27,28,29,31) in SOP form. (8M+7M)

4. a) With the help of logic diagram explain a ripple adder/ subtractor using 2's compliment system.
   b) Design a full subtractor using AND, OR, NOT gates (9M+6M)

5. a) Design a 4 to 1 MUX using a 2 to 4 decoder and basic gates
   b) Design a BCD to decimal decoder. (7M+8M)

6. A combinational circuit is defined by the functions
   $F_1=\sum m(3,5,6,7)$ $F_2=\sum m(0,2,4,7)$
   Implement the circuit with a PLA having 3 inputs, 4 products terms and 2 outputs (15M)

7. a) Define the following terms of flip-flops
   i) Hold time ii) setup time iii) propagation delay time
   b) Design a sequence detector with over lapping, the sequence is 10110.Use JK flip-flop. (6M+9M)

8. a) Design a modulo 12 up synchronous using T-flip-flops and draw the circuit diagram.
   b) Compare synchronous and asynchronous sequential circuits. (10M+5M)
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