Code: 9A04704

1

B. Tech IV Year II Semester (R09) Regular Examinations, March/April 2013

DSP PROCESSORS & ARCHITECTURES

(Electronics & Instrumentation Engineering)

Time: 3 hours Max. Marks: 70

Answer any FIVE questions

All questions carry equal marks

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1 (a) Explain memory access schemes in P-DSP's.

(b) A DSP has a circular buffer with the start and the end addresses as 0200h and 020Fh, respectively. What would be the new values of the address pointer of the buffer if, in the course of address computation, it gets updated to (a) 0212h, (b) 01FCh?

2 (a) Explain the DSP computational errors involved in multiplications or MAC operations.

(b) Calculate the dynamic range and precision of each of the following number representation formats:

(i) 24-bit, single precision, fixed point format

(ii) 48-bit, double precision, fixed point format

(iii) A floating point format with a 16-bit mantissa and an 8-bit exponent.

3 (a) Draw and explain the structure of 4 X 4 Braun multiplier.

(b) Explain the memory architecture required for a DSP device to implement 2^M - point FET.

4 (a) Draw and explain the functional diagram of the barrel shifter of the TMS320C54xx processors.

(b) Write a TMS320C54xx program to mark the lower 6-bits of a word stored in the data memory and write the modified word back at the same location.

5 (a) Explain how adaptive filter coefficients can be updated on line to counter varying signal distortions.

(b) Write a program to show how to implement an interpolating FIR filter. The filter length is 15 and the interpolating factor is 5.

6 Write a program to compute 8-point DFT using DIT FET algorithm. Also compute signal spectrum using the transformed data.

7 (a) How does DMA help in increasing the processing speed of a DSP processor?

(b) Design a circuit to interface 64k words of the program memory space from OFFFFFh to OFOOOOh for the TMS320C5416 processor using 16k X 16 memory chips.

8 (a) Give the comparison of the features of FPGA based DSP systems with P-DSPs.

(b) Write an overview of open multimedia applications platform (OMAP).

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DSP PROCESSORS & ARCHITECTURES

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1 (a) What are the special addressing modes in P-DSPs and explain them?
(b) Write about VLIW architecture of P-DSP's.

2 (a) Compute the dynamic range and the percentage resolution for a block floating point format with a 4-bit exponent used in a 16-bit fixed point processor.
(b) Explain different number formats for signals and coefficients in DSP system.

3 (a) Explain the basic features that should be provided in the DSP architecture to be used to implement the following nth order FIR filter $y(n) = \sum_{i=0}^{N-1} h(i)\, x(n-i);\ n = 0,1,2 \ldots$ $x(n)$ is input sample, $y(n)$ is the output sample, $h(i)$ the filter coefficient, $x(n-i)$ is the i/p sample i samples earlier than $x(n)$.
(b) Write about on-chip memory of DSP.

4 (a) Explain six stage pipeline of TMS 320C54xx execution.
(b) Explain program control operations of TMS320C54xx processor with example each.

5 (a) Explain memory organization for matrix multiplication of a 3×4 matrix with 4×3 matrix in DSP.
(b) Explain how decimation filter in used to decrease the sampling rate in P-DSPs.

6 (a) Write a programme to compute a FFT for any number of points that are powers of 2 for TMS 320C54xx DSP.
(b) With an example explain Bit-reversed index generation for an 8-point DFT computation of DSP.

7 (a) What is the range of addresses that can be decoded if A19 is pulled low in a processor with 20 address lines?
(b) For TMS 320C54xx DSP operating at a clock frequency of 100MHz, how many 16-bit data elements can be transferred between two internal memory locations per second in the DMA mode?

8 Write a short note on:
(i) Development tools for programmable DSPs.
(ii) Design flow for an FPGA based system design.

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DSP PROCESSORS & ARCHITECTURES

(Electronics & Instrumentation Engineering)

Time: 3 hours Max. Marks: 70

Answer any FIVE questions

All questions carry equal marks

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1 (a) Explain the architectural feature of pipelining to increase the speed of DSP.
(b) Implement an $8 \text{ X } 8$ multiplier using $4 \text{ X } 4$ multiplex as the building blocks.

2 (a) Explain sources of error in DSP implementation.
(b) Show that the dynamic range of a signal increases by 6dB for each additional bit used to represent its value.

3 (a) Explain the features for external interfacing of DSP.
(b) Implement parallelism of an 8-tap FIR filter using two MAC units.

4 (a) Draw and explain the block diagram of the indirect addressing mode of TMS320C54xx processor using dual memory operands.
(b) What are the data addressing modes of TMS 320C54xx processor?

5 (a) With an example explain how to implement an adaptive filter to implement a 9-tap adaptive filter.
(b) Determine the linearly interpolated sequence from the given sequence, $x(n) = [0\ 4\ 8\ 12\ 16\ 12\ 8\ 4\ 0]$ for an interpolation factor of 3. What interpolating sequence h(n) can achieve the specified interpolation?

6 (a) Explain a general DIT FFT butterfly computation.
(b) Draw and explain the signal flow graph for an 8-point DFT computation.

7 (a) What are the various classifications of interrupts for the TMS 320C5416 processor?
(b) How many address lines are required to access all locations of an $16\text{K X } 16$ SRAM?

8 Write a short note on:
(i) FPGA based DSP system design
(ii) Development tools for FPGAs

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4

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DSP PROCESSORS & ARCHITECTURES

(Electronics & Instrumentation Engineering)

Time: 3 hours Max. Marks: 70

Answer any FIVE questions

All questions carry equal marks

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1 (a) Explain on chip peripherals used to interfacing with external devices.

(b) Explain the operation of the following MAC instruction.

(i) $\mathrm{MAC} * \mathrm{AR5}+,\ \#\ 1234\mathrm{h}, \mathrm{A}$

(ii) $\mathrm{MAC} * \mathrm{AR3}-,\ *\mathrm{AR4}+, \mathrm{B}, \mathrm{A}$

2 (a) Explain quantization error in truncation A/D converter with suitable diagram.

(b) Evaluate the performance measure SNR of A/D converter with $\mathrm{b} = 14$.

3 (a) Compute the sequence in which the input data should be ordered for a 16-point DIT FFT.

(b) Explain basic architectural features of P-DSPs.

4 (a) Draw and explain the block diagram of the circular addressing mode for TMS320C54xx processor.

(b) Mention load and store operations of TMS 320C54xx processor with example each.

5 (a) Determine the value of each of the following 16-bit numbers represented using the given Q-notation.

(i) 4400h as a Q0 number

(ii) 4400h as a Q15 number

(iii) 4400h as a Q7 number

(b) Explain how interpolation filter is used to increase the sampling rate.

6 (a) What minimum size FFT must be used to compute a DFT of 40 points? What must be done to the samples before the chosen FFT is applied?

(b) Derive the optimum scaling factor for the DIF FFT butterfly.

7 (a) Up to what limit can the program memory be extended in a processor with 20 address lines. How must the extended memory be organized for addressing by a C54xx processor?

(b) How does the interrupt handling in the TMS 320C54xx DSP differ for a software and hardware interrupt?

8 Write about

(i) CAD tools for FPGA based system design

(ii) Soft core processors

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