Code: R7420406

R7

B.Tech IV Year II Semester (R07) Supplementary Examinations, March/April 2013

DSP PROCESSORS & ARCHITECTURES

(Common to ECE and EIE)

Time: 3 hours Max Marks: 80

Answer any FIVE questions

All questions carry equal marks

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1 (a) Explain the terms thermal drift, reliability and repeatability pertaining to digital signal processing.

(b) Determine the impulse response coefficients of a digital low power filter with $H(e^{J\,2\pi+Ts}) = 1$ for $f < f_c\ and = 0, for\ f_c < f < {}^{f_s}/_{2}$.

2 Explain in detail about various sources of error in DSP implementations with suitable examples.

3 (a) Explain about the Von Neumann architecture for DSP processors.

(b) What are the special addressing modes in P-DSP's? Explain.

4 (a) Explain about pipe line programming models with suitable example.

(b) Write short notes on interlocking mechanism related to execution control and pipelining.

5 Explain about TMS320C54XX processor buses, internal memory organization and CPU.

6 (a) Give the functional diagram of TMS320C54XX multiplier and adder units and explain the same.

(b) What are the different addressing modes of C54X processor? Explain giving examples.

7 Explain about an 8 point FFT implementation on the TMS320C54XX DSP processor.

8 (a) Explain the CODEC programming and Q notation.

(b) Explain the implementation of DSP algorithms for IIR filters.

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