

Code: R7420404

**R7****B.Tech IV Year II Semester (R07) Supplementary Examinations March/April 2013****DIGITAL DESIGN THROUGH VERILOG**  
(Common to ECE and ECC)

Time: 3 hours

Max Marks: 80

Answer any FIVE questions  
All questions carry equal marks

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- 1 (a) Explain bottom – up design methodology with example.  
(b) Explain HDL advantages compared to traditional schematic based design.  
(c) Explain typical design flow of HDL's
- 2 (a) Design a module for conversion of 8 bit number into its respective BCD's.  
(b) Write verilog module for addition of 32 bit words.
- 3 (a) Design a verilog code for a counter realized using if else construct.  
(b) Design a verilog code for 2 to 4 demux through procedural continuous assignment.
- 4 (a) Design verilog module for CMOS inverter.  
(b) Design verilog module for 3 input CMOS NAND gate.
- 5 (a) Design verilog module for up down counter module using specify parameters.  
(b) Design 1 bit full subtractor using XOR, AND, OR gates.
- 6 (a) Explain PLA realization of dice game controller.  
(b) Write HDL code for counter in dice game.
- 7 (a) Explain about programmable interconnects – XC 4000.  
(b) Explain about dice roll controllers.
- 8 (a) Design and explain block diagram of RAM system.  
(b) Design HDL module for UART transmitter.

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