Code: 9A04504 **R9**

B.Tech III Year I Semester (R09) Supplementary Examinations, May 2013

DIGITAL IC APPLICATIONS

(Electronics and Communication Engineering)

Time: 3 hours Max Marks: 70

Answer any FIVE questions

All questions carry equal marks

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1 (a) Explain the effect of floating inputs on CMOS gate.
(b) Explain how a CMOS device is destroyed.
(c) What is the difference between transmission time and propagation delay? Explain these two parameters with reference to CMOS logic.

2 (a) Compare CMOS, TTL and ECL with reference to logic levels, DC noise margin, propagation delay and fan-out.
(b) Draw the circuit diagram of basic CMS gate and explain the operation.

3 (a) Explain with an example the syntax and the function of the following VHDL statements:
(i) Process statement. (ii) Case statement.
(b) Explain implicit and explicit visibility of a library in VHDL.

4 (a) Write the data flow style VHDL program for this IC.
(b) Write a process based VHDL program for the prime-number detector of 4-bit input and explain the flow using logic circuit.

5 Draw the logic diagram of 74X283 and explain its operation and write a VHDL code in data flow model.

6 Draw the logic diagram of 74X283 and explain its operation and write a VHDL code in data flow model.

7 (a) Design a conversion circuit to convert a SR flip-flop to JK flip flop.
(b) Write a VHDL code for a SR flip-flop in behavioral model.

8 Determine the ROM size needed to realize the combinational logic function performed by each of the following MSI parts 74X49, 74X139, 74X153, 74X257, 74X381, 74X682.

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