

R07
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**Code: R7210504**

B.Tech II Year I Semester (R07) Supplementary Examinations, May 2013

**DIGITAL LOGIC DESIGN**  
(Common to CSE, IT & CSS)

Time: 3 hours

Max. Marks: 80

Answer any FIVE questions  
All questions carry equal marks

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- 1 (a) Convert the following numbers with the given radix to decimal.
  - (i)  $2345_5$
  - (ii)  $2345_7$
  - (iii)  $2345_{11}$ .(b) Design a BCD to excess-3 code converter using minimum number of NAND gates.
- 2 (a) Explain any two Boolean functions and prove them. Explain the truth tables of X-OR, NAND, NOR gates.  
(b) Explain the differences among a truth table, a state table, a characteristic table, and an excitation table with examples.
- 3 (a) Reduce the following Boolean expressions to three literals.  
 $A'C' + ABC + AC'$ .  
(b) Minimize the following function.  $F = (0, 2, 4, 8, 9, 12, 14)$ . Show the gating circuit after minimization.
- 4 (a) Implement full subtractor using NAND gates only.  
(b) Design a full adder circuit using 2 half adders.
- 5 (a) Explain the design of sequential circuit with an example. Show the state reduction, state assignment.  
(b) Explain briefly the analysis of clocked sequential circuits.
- 6 (a) Design a 8-bit ring counter.  
(b) Design a 4-bit universal shift-register that has all the capabilities.
- 7 (a) Explain the block diagram of a memory unit. Explain the read and write operation a RAM can perform.  
(b) Explain about read only memory in detail.
- 8 (a) Draw and explain the gated-latch logic diagram.  
(b) Explain error detection and correction read only memory.

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