Code No: R22043 **R10** SET - 1

II B. Tech II Semester, Supplementary Examinations, Dec – 2012
ELECTRONIC CIRCUIT ANALYSIS
(Com. to ECE, EIE)

Time: 3 hours Max. Marks: 75

Answer any **FIVE** Questions
All Questions carry **Equal** Marks
~~~~~~~~~~~~~~~~~~~~~~~~

1. a) Derive the equations for voltage gain, current gain, input impedance and output admittance for a BJT-CC amplifier using low frequency h-parameter model.
   b) Draw the small signal equivalent circuit of FET-CS amplifier and derive the expression for voltage gain. (8M+7M)

2. a) Calculate the Voltage gain, Input Impedance and Output Impedance of a Voltage Series Feedback amplifier having an Open-loop gain A=300, R_i=1.5KΩ, R_o=50KΩ and ß= -1/20.
   b) Explain the general characteristics of negative feedback amplifiers. (7M+8M)

3. a) Perform the generalized analysis of LC oscillators with suitable block diagram and obtain the circuit diagrams of Hartley and Colpitts oscillators.
   b) The ac equivalent circuit of a Crystal has the Values: L=3 H, C_S=0.005pF, R= 2KΩ and C_m=10 pF. Determine the series and parallel resonant frequencies of the Crystal. (8M+7M)

4. a) Perform the analysis of two stage RC Coupled JFET-CS Amplifier circuit.
   b) Draw the circuit diagram for differential amplifier and perform the analysis with its equivalent circuit. (8M+7M)

5. a) Discuss about Hybrid-π capacitances. How do Hybrid-π parameters vary with temperature?
   b) Following measurements of a certain transistor are available at room temperature and with I_C = 5 mA, h_{fe} = 100, h_{ie} = 0.62 KΩ. Short circuit current gain = A_{IS} = 10 at 10MHz. $C_{b'c}$ = 3_{pF}. Calculate f_T and f_{β}. (8M+7M)

6. a) Ideal class-B transformer-coupled audio amplifier is fed from 20V DC. Transformer ratio is $\frac{N_p}{N_s} = 4$. A 4 ohm speaker is connected to load. Calculate:
   i) Maximum signal power delivered to load. ii) Power dissipation rating to each transistor.
   iii) Maximum excitation current at input if transfer characteristic is linear (h_{fe} = 20).
   b) Show that class B push pull amplifiers exhibit half wave symmetry. (7M+8M)

7. a) Derive the expression for the gain of a single-tuned capacitance coupled amplifier. Discuss about its Selectivity.
   b) Draw and explain the circuit diagram for single tuned capacitive coupled amplifier and derive the expression for (A/A_{reso}) . (8M+7M)

8. a) Draw the circuit and explain how short circuit over load protection is provided in Voltage Regulators circuits.
   b) Design a zener-shunt regulator with the specifications using a zener diode with V_Z = 10V. Input supply voltage varies from 15V to 25V and the load current varies between 0 and 15 mA. Also determine the line and load regulation. (8M+7M)
~~~~~~~~~~~~~~~~~~~~~~~~

Code No: R22043 **R10** SET - 2

II B. Tech II Semester, Supplementary Examinations, Dec – 2012
ELECTRONIC CIRCUIT ANALYSIS
(Com. to ECE, EIE)

Time: 3 hours Max. Marks: 75

Answer any **FIVE** Questions
All Questions carry **Equal** Marks
~~~~~~~~~~~~~~~~~~~~~~~~

1. a) Perform the generalized analysis of single stage BJT-CE amplifier using h-parameter model.
   b) Draw the Small Signal model of JFET-CS amplifier and derive the expressions for the voltage gain, the output impedance and the input impedance. (8M+7M)

2. a) What are the different types of negative feedback? Explain how the input and output impedances of an amplifier are affected by the different types of negative feedback.
   b) The open loop voltage gain of the amplifier of an amplifier is 50. Its input impedance is 1kΩ. What will be the input impedance where a negative feedback of 10% is applied to the amplifier? (10M+5M)

3. a) Draw the circuit of Hartley oscillator and explain its working. Derive the expressions for frequency of oscillation and condition for starting of oscillation.
   b) Draw the equivalent circuit of a quartz crystal. What makes the quartz produce stable oscillations? (10M+5M)

4. a) Draw the circuit diagram of cascode-transistor amplifier Circuit and analyze its performance.
   b) Draw and explain the working of two-stage BJT-RC Coupled amplifier. Derive the expression for its voltage gain. (7M+8M)

5. a) Explain the concept of CE short circuit current gain with its equivalent circuit. Derive the necessary expressions.
   b) The following low-frequency parameters are available for a transistor at

   I_{CQ} = 5 mA

   h_{ie} = 1K, h_{fe} = 100 h_{oe} = 4 x 10^{-5} A/V

   h_{re} = 10^{-4} C_{ob} = 2 pF f_T = 10 MHz

   Compute the values of hybrid-π parameters at room temperature. (8M+7M)
~~~~~~~~~~~~~~~~~~~~~~~~

Code No: R22043 **R10** SET - 2

6. a) Derive the expression for maximum value of conversion efficiency of Class A Power amplifier.

   b) A power transistor is to be used as a class A transformer coupled amplifier and is to deliver a maximum of 5W to a 4 ohm load. Operating point is adjusted for symmetrical clipping with collector supply voltage of 20V. Assume ideal characteristics with V_{min} = 0V. Calculate
   (i) Transformer turns ratio (ii) Peak collector current
   (iii) Operating point values of I_{CQ} and V_{CEQ} (iv) Power dissipation rating of transistor
   (v) Collector circuit efficiency (7M+8M)

7. a) Draw the circuit diagram of a double-tuned amplifier and explain its working and derive the expression for I_2 max.

   b) A parallel resonant circuit comprises of an inductor (having inductance of 1mH and resistance of 10Ω) and a parallel capacitor of 100 pF.
   Calculate: (i) Resonant frequency, ignoring the resistance
   (ii) Resonant frequency, considering the resistance (iii) Q-factor.
   (iv) Impedance at resonant frequency. (8M+7M)

8. a) Define the terms i) Load Regulation ii) Line Regulation iii) Ripple Rejection and iv) Temperature Stability pertaining to Voltage Regulators.

   b) A shunt regulator utilizes a Zener diode whose voltage is 5.1 V at 50 mA and whose r_z = 7Ω. The diode is fed from a 15V DC supply through a 200 Ω resistor. What is the output voltage at no load? Find the line and load regulations. (8M+7M)

Code No: R22043 **R10** SET - 3

II B. Tech II Semester, Supplementary Examinations, Dec – 2012
ELECTRONIC CIRCUIT ANALYSIS
(Com. to ECE, EIE)

Time: 3 hours Max. Marks: 75

Answer any **FIVE** Questions
All Questions carry **Equal** Marks
~~~~~~~~~~~~~~~~~~~~~~~~

1. a) Draw the small signal model of FET for low frequency region and compare with the relevant BJT model and explain.
   b) Derive the equations for voltage gain, current gain, input impedance and output impedance for a BJT-CB amplifier using approximate h-parameter model. (7M+8M)

2. a) Explain the concept of feedback and present the feedback topologies.
   b) A single stage CE amplifier has a Voltage gain of 600 without feedback. When feedback is employed, its gain reduces to 50. Calculate the percentage of the output which is fed back to the input. (8M+7M)

3. a) Explain the working of Wien Bridge Oscillator using BJT. Also derive the expression for the frequency of Oscillation.
   b) Design a RC phase-shift oscillator, which has the following specifications: h_{fe}=200, I_E=1.5mA, S=8, V_{CC}=12V and oscillation frequency expected is 500Hz. (8M+7M)

4. a) Draw the circuit for Darlington pair amplifier and derive the expressions for A_I, Av, R_i and $R_{o.}$
   b) Design a two-stage CE-CE amplifier for the given data. h_{fe1}=h_{fe2}=180, R_L=1KΩ I_{E1}=I_{E2}=1mA, S=3, V_{CC}=12V, f=100Hz. Assume identical transistors. (8M+7M)

5. a) Derive the expressions for resistive parameters of Hybrid-π model in terms of low frequency h-parameters.
   b) Following measurements of a certain transistor are available at room temperature and with Ic = 5 mA, V_{CE}=10V, h_{fe} = 100, h_{ie} = 600Ω. [A_{ie}] = 10 at 10MHz. C_c = 3pF. Calculate $f_{\beta,}$ $f_{T,}$ $C_{e,}$ $r_{bb'e}$ and $r_{bb'}$. (8M+7M)

6. a) Write short notes on Heat Sinks used in power amplifiers and also give the classification.
   b) Explain Class D and Class S power amplifiers. Mention their salient features and applications. (7M+8M)

7. a) Draw the circuit diagram of a double-tuned amplifier and explain different stages of simplification of its equivalent circuit.
   b) A circuit is resonant at 455 kHz and has a 10 kHz bandwidth. The inductive reactance is 1255Ω. What is the parallel impedance of the circuit at resonance? (8M+7M)

8. a) Define different performance parameters of a voltage regulator and explain their importance.
   b) A series regulator has stability factor of $6*10^{-3}$ and output resistance of 10^{-4} ohms. Calculate the change in output voltage when
   i) Unregulated input d.c voltage varies by 10V. ii) Load current varies by 250mA. (8M+7M)
~~~~~~~~~~~~~~~~~~~~~~~~

Code No: R22043 **R10** SET - 4

II B. Tech II Semester, Supplementary Examinations, Dec – 2012
ELECTRONIC CIRCUIT ANALYSIS
(Com. to ECE, EIE)

Time: 3 hours Max. Marks: 75

Answer any **FIVE** Questions
All Questions carry **Equal** Marks
~~~~~~~~~~~~~~~~~~~~~~~~

1. a) Draw the Small Signal model of Common-Drain JFET amplifier and derive the expressions for the voltage gain, the output impedance and the input impedance.
   b) Consider a single stage CE amplifier with R_s = 1KΩ, R_e = 50 KΩ, R_2 = 2KΩ, R_c = 1K, R_L = 1.2KΩ, h_{fe} = 50, h_{oe} = h_{re} = 0. h_{ie} = 1.1KΩ. Determine A_i, R_o, A_v and power gain using exact method of Analysis. (8M+7M)

2. a) Enumerate the effects of negative feedback on the various characteristics of the amplifier.
   b) The open loop gain of an amplifier is 50Db. A negative feedback of feedback factor 0.004 is applied to it. If the open loop gain is thereby reduced by 10% find the change in the overall gain. (10M+5M)

3. a) Derive the expression for the frequency of oscillation and the minimum gain required for sustained oscillations of the RC phase shift oscillator using BJT.
   b) A crystal has the following parameters:
   L=0.33 H, Cs=0.0655 pF, Cp=1.0pF and R=5.5KΩ .
   Find the series resonant frequency and Q-factor of the crystal. (10M+5M)

4. a) Perform the Analysis of Boot-Strapped Emitter follower Circuit.
   b) Three identical non-interacting amplifier stages are cascaded with an overall gain of 0.3dB down at 50 kHz compared to midband. Calculate the upper cutoff frequency of the individual stages. (8M+7M)

5. a) Draw the equivalent circuit of hybrid-π model and derive the expressions for Hybrid-π impedances in terms of low frequency h-parameters.
   b) The following low-frequency parameters are available for a transistor at
   I_C =10 mA, V_{CE}=10V and at room temperature
   h_{ie} = 500Ω h_{fe} = 100 h_{oe} = 10^{-5} A/V h_{re} = 10^{-4}
   At the same Operating point, f_T=50 MHz and C_{ob} = 3 pF Compute the values of all the hybrid-π parameters. (8M+7M)

6. a) Draw the circuit diagram of class-B push pull amplifier and explain the operation.
   b) Deduce the expression which gives the relationship between maximum collector dissipation and maximum power output of class-B push pull amplifier. (8M+7M)

7. a) Draw the circuit diagram of double-tuned amplifier and simplify the same with its equivalent circuit.
   b) Write notes on quality factor and bandwidth of parallel tuned circuit. (8M+7M)

8. a) Draw and explain the circuit diagram of series type voltage regulator and present its characteristics.
   b) Design a voltage regulator circuit to give output voltage adjustable from 10 to 15 volts. Maximum output current is 100mA and input voltage is 20volts. (8M+7M)
~~~~~~~~~~~~~~~~~~~~~~~~