

Code No: L0421

**R07**

**Set No. 1**

**IV B.Tech II Semester Supplementary Examinations, July/Aug 2012**  
**EMBEDDED AND REAL TIME SYSTEMS**  
**(Common to Electronics & Communication Engineering and Electronics & Instrumentation Engineering)**

**Time: 3 hours**

**Max Marks: 80**

**Answer any FIVE Questions**  
**All Questions carry equal marks**

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1. (a) What is an Embedded System? Differentiate between a general purpose computing system and an embedded system?  
(b) what are the designer trade- offs among the advantages and disadvantages of various available processor technologies and IC technologies? [8+8]
2. (a) Explain briefly how to test and debug an Embedded System.  
(b) Compare two different vendor microprocessors of your choice and explain all aspects related to them with neat diagram? [8+8]
3. (a) Give pseudo-code for a pair of functions implementing the send and receive communications constructs. You may assume that mutex and condition variables are provided.  
(b) List three requirements of real-time systems and briefly describe each of them. Give examples of actual real-time systems to support your arguments. [8+8]
4. (a) Explain about USB.  
(b) Explain briefly about RS232 and UART. [8+8]
5. With suitable examples explain how do you : [5+5+6]  
(i) Acquire a Semaphore (ii) Release a Semaphore (iii) Query a Semaphore.
6. With suitable examples explain how to  
(i) Send a signal to another Task (ii) Block a signal from being delivered.  
(iii) Unblock a blocked signal. [5+5+6]
7. (a) Explain about the issues involved in synchronization of data between the hand-held computers and desktop computers.  
(b) Explore the standardization activities for data synchronization. [8+8]
8. (a) Describe the new challenges created by 'cores' for processor developers as well as users.  
(b) Show the correspondence of these types of cores with Gajskis Y- Chart. [8+8]

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1. (a) Explain why NAND and NOR gates are more common than AND and OR gates?
- (b) Design a 3X8 decoder, start from a truth table use K - maps to minimize logic and draw the final circuit? [4+12]
2. Create a table listing the address spaces for the following address sizes:
  - (a) i. 8 - bit
  - ii. 16 - bit
  - iii. 24 - bit
  - iv. 32 - bit
  - (b) Explain the following
    - i. Data path
    - ii. Control unit. [2+2+2+2+4+4]
3. (a) Explain briefly about Synchronization among Processes.
- (b) Write a note on Scheduling Processes. [8+8]
4. Write a note on the following topics
  - (i) L2CAP      (ii) SDP      (iii) RFCOMM      (iv) TCS. [4+4+4+4]
5. What are the Kernel services in any operating system. Briefly explain any three such services. [16]
6. With suitable examples explain how to :
  - (a) Set an event flag
  - (b) Clear an event flag
  - (c) Query an event flag. [5+5+6]
7. List the various Open source embedded operating systems and explain their features. [16]
8. Explain the impact of complexity of the logic on logic synthesis. [16]

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**R07****Set No. 3**

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1. (a) Explain about sequential logic design.  
 (b) Explain RT-Level custom single purpose processor design. [8+8]
2. (a) How an Embedded System designer selects a microprocessor?  
 (b) Suppose that your system has two ROM chips and two RAM chips whose sizes and addresses are as shown in the following table. Design the part of the circuit that takes the appropriate address lines as inputs and produce the chip enable signals for each of these four memory chips. [8+8]

	Size	Low Address	High Address
ROM	128 KB	0x00000	0x1FFFF
ROM	128 KB	0x20000	0x3FFFF
RAM	64 KB	0x80000	0x8FFFF
RAM	64 KB	0x90000	0x9FFFF

3. How numerous operations permitted by the concurrent process model are implemented by using single or general - purpose processors? [16]
4. (a) Explain all about the Ethernet LAN Protocol Architecture.  
 (b) Explain all about the IEEE 1394 Protocol Architecture. [8+8]
5. (a) Explain Task scheduling and give some examples  
 (b) Explain about the following scheduling algorithms  
 (i) First-in-First-out. (ii) Round-Robin with priority. [8+8]
6. With suitable examples explain how to  
 (i) Send a signal to another Task (ii) Block a signal from being delivered.  
 (iii) Unblock a blocked signal. [5+5+6]
7. (a) Explain the difference among various types of off - the shelf operating systems.  
 (b) Explain any three POSIX system calls with proto-type and give example for each. [10+6]
8. With examples explain the Two-level and multi-level logic minimization With respect to synthesis process. [16]

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1. (a) Explain about sequential logic design.  
(b) Explain RT-Level custom single purpose processor design. [8+8]
2. (a) Illustrate how program and data memory fetches can be overlapped in a Harvard architecture.  
(b) Explain briefly how to test and debug an Embedded System. [8+8]
3. (a) Compare State Machine and Sequential Program Models.  
(b) Give pseudo-code for a pair of functions implementing the send and receive communications constructs. You may assume that mutex and condition variables are provided. [8+8]
4. What are Bluetooth devices? Explain how they can be used to setup Personnel Area Networks? [16]
5. (a) Explain about context switching with examples.  
(b) Explain about the following scheduling algorithms  
    i. Round -Robin  
    ii. Non primitive multitasking. [8+8]
6. With suitable examples explain how to  
(i) Send a signal to another Task      (ii) Block a signal from being delivered.  
(iii) Unblock a blocked signal. [5+5+6]
7. (a) What is Tornado development environment? Explain with neat block Diagram.  
(b) Explain the following states of VxWorks tasks  
    i. Ready  
    ii. Pending  
    iii. Delay  
    iv. Suspend [8+8]
8. List and describe three general approaches to improve designer productivity. [16]

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