Code No: N0522 **R07**

Set No. 1

IV B.Tech. I Semester Regular Examinations, November, 2012 EMBEDDED SYSTEMS

(Common to Computer Science & Engineering and Information Technology)
Time: 3 Hours

Max Marks: 80

Answer any FIVE Questions All Questions carry equal marks

- 1. a) Briefly describe the differences between requirements and specifications.
 - b) Explain the structural description of system design.

[4+12]

- 2. a) Explain the configuration of different port pins as inputs or outputs using relevant diagrams and explain the features of each port of 8051 microcontroller.
 - b) Explain the concept of memory banks using relevant diagrams.

[10+6]

- 3. a) Explain external addressing using MOVX and MOVC.
 - b) Explain all possible addressing modes for data exchange instruction.
 - c) Write an assembly language program to exchange the contents of SP and PSW.

[6+6+4]

- 4. a) Explain the operation performed by the following instructions using an example and indicate the possible flags to be affected.
 - i) ADDC
- ii) MUL

iii) RLC

- iv) ACALL sadd.
- b) Random numbers are placed in registers R2 and R5. Write an assembly language program to increment R2 and decrement R5 until they are equal.
- c) Write an assembly language program to get the contents of DPTR to PC. [8+6+2]
- 5. a) Explain interfacing of 8051 microcontroller with A/D converter using a relevant circuit diagram.
 - b) Write a program to interface 8051 microcontroller with A/D converter.

[8+8]

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Set No. 1

- 6. a) Explain shared data problems.
 - b) What is a reentrant function? Check whether the function shown below is reentrant.

c) Compare RTOS with a standard operating system.

[8+4+4]

- 7. a) Discuss the methods and strategies to save memory space in an embedded system.
 - b) Describe the operation of ROM emulators.
 - c) Write notes on cross-assemblers and tool chains.

[8+4+4]

- 8. a) Discuss the features, examples and an application of internet enabled embedded system.
 - b) Describe the structure of I²C bus system.
 - c) Describe the data frame format of a CAN bus.
 - d) What is the requirement of distributed embedded system.

[5+4+4+3]

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R07

Set No. 2

IV B.Tech. I Semester Regular Examinations, November, 2012 EMBEDDED SYSTEMS

(Common to Computer Science & Engineering and Information Technology)
Time: 3 Hours

Max Marks: 80

Answer any FIVE Questions All Questions carry equal marks

- a) Briefly describe the differences between specification and architecture.
 b) Explain the behavioral description of system design. [4+12]
 a) Draw the 8051 block diagram and explain the oscillator circuit and timing.
- b) Draw the contents of IE and IP registers explain how different interrupt functions are controlled by IE and IP registers. [8+8]
- 3. a) Explain PUSH and POP instructions considering an example stack.
 - b) Write an assembly language program to copy program bytes 0100h to 0102h to internal RAM locations 20h to 22h.
 - c) Write an assembly language program to copy the external code byte at address 007Dh to the SP. [6+6+4]
- 4. a) Explain the operation performed by the following instructions using an example and indicate the possible flags to be affected.
 -) DA ii) CPL A
- iii) RRC
- iv) AJMP sad
- b) Random unsigned numbers are placed in registers R0 to R4. Write an assembly language program to find the largest and place the result in register R6. [8+8]
- 5. a) Explain interfacing of 8051 microcontroller with D/A converter using a relevant circuit diagram.
 - b) Write a program to interface 8051 microcontroller with D/A converter.

[8+8]

[16]

[8+8]

- 6. Write in detail about Semaphores and shared data .
- 7. a) Explain the goals of typical testing process.b) Discuss the methods and strategies to save power in an embedded system.
- 8. With reference to design of elevator controller
 - a) Write the theory of operation and requirements
 - b) Write the specifications
 - c) Discuss the architecture
 - d) Brief testing.

[5+5+4+2]

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Set No. 3

IV B.Tech. I Semester Regular Examinations, November, 2012 EMBEDDED SYSTEMS

(Common to Computer Science & Engineering and Information Technology)
Time: 3 Hours

Max Marks: 80

Answer any FIVE Questions All Questions carry equal marks

- 1. a) Describe the characteristics of embedded computing system applications.
 - b) Explain the architecture design of an embedded system including hardware and software architectures using an example. [6+10]
- 2. a) Explain different serial data transmission modes of 8051 microcontroller.
 - b) Explain internal RAM organization of 8051 microcontroller.

[10+6]

- 3. a) Explain direct and indirect addressing modes using relevant examples.
 - b) Write an assembly language program to exchange both lower nibbles of registers R0 and R1.
 - c) Write an assembly language program to store DPTR in external RAM locations 0123h (DPL) and 0124h (DPH). [8+4+4]
- 4. a) Explain the operation performed by the following instructions using an example and indicate the possible flags to be affected.
 - i) SUBB
- ii) CPL C
- iii) SETB C
- iv) CJNE @Rp,#n,radd
- b) Write an assembly language program to put a random number in register R3 and decrement it till it equals E1h
- c) Write an assembly language program to count the number of zeros in any number in register R3 and put the result in register R5. [8+4+4]
- 5. a) Explain interfacing of 8051 microcontroller using any key board configuration using relevant circuit diagram.
 - b) Write a program to interface 8051 microcontroller with D/A converter. [8+8]

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Set No. 3

- 6. a) Define task and explain different states in which a task can be in an RTOS.
 - b) i) Explain the role of a scheduler in a RTOS environment.
 - ii) How does a scheduler know when a task is blocked or unblocked?
 - iii) How does a scheduler handle when all tasks are blocked
 - iv) How does a scheduler handle when two tasks with same priority are ready. [8+8]
- 7. a) Describe the operation of PROM programmers.
 - b) Write notes on cross-compilers.
 - c) Write notes on encapsulating semaphores.

[5+6+5]

- 8. Explain the following with reference to a CAN bus
 - a) Physical and Electrical organization
 - b) Data frame format
 - c) Bus arbitration
 - d) Error handling
 - e) Architecture of a CAN controller

[3+4+3+3+3]

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Set No. 4

IV B.Tech. I Semester Regular Examinations, November, 2012 EMBEDDED SYSTEMS

(Common to Computer Science & Engineering and Information Technology)
Time: 3 Hours

Max Marks: 80

Answer any FIVE Questions All Questions carry equal marks

- 1. a) Compare and contrast top-down and bottom-up design.
 - b) Draw flow chart indicating the major levels of abstraction in the design process and explain in detail the requirements and specification levels. [4+12]
- 2. a) Explain different timer modes of 8051 microcontroller.
 - b) What are different flags available in 8051 microcontroller? Indicate them in PSW register and explain the role of each bit in it. [10+6]
- 3. a) Explain immediate and register addressing modes using relevant examples.
 - b) Write an assembly language program to exchange the contents of B register and external RAM address 02CFh.
 - c) Write an assembly language program to copy the data at internal RAM location F1h to R0 and R3. [6+6+4]
- 4. a) Explain the operation performed by the following instructions using an example and indicate the possible flags to be affected.
 - i) ORL
- ii) DIV
- iii) CJNE
- iv) JNB b, radd
- b) Explain the ranges of different jump instructions.
- c) Write an assembly language program to put a random number in register R3 and increment it till it equals E1h. [8+4+4]
- 5. a) Explain interfacing of 8051 microcontroller with seven segment display using a relevant circuit diagram.
 - b) Write a program to interface 8051 microcontroller with seven segment display. [8+8]

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Set No. 4

6. a) Compare different methods of protecting shared data.

- b) Explain the rules which the interrupt service routines must follow in most RTOS environments.
- c) Compare different methods for inter task communication.

[5+6+5]

- 7. a) Describe the operation of in-circuit emulators.
 - b) Discuss the hard-real time scheduling considerations.
 - c) Write notes on encapsulating queues.

[6+6+4]

- 8. a) Explain the structure of an I²C bus system.
 - b) Explain the features of electrical interface to I²C bus.
 - c) Explain typical bus transaction on the I²C bus using state transition graph, considering a format for address transmission.

[4+4+8]