Code No: V0222 **R07** SET - 1

II B. Tech II Semester, Supplementary Examinations, April/May – 2013
LINEAR DIGITAL IC APPLICATIONS
(Electrical and Electronics Engineering)

Time: 3 hours Max. Marks: 80

Answer any **FIVE** Questions
All Questions carry **Equal** Marks
~~~~~~~~~~~~~~~~~~~~~~~~~~

1. a) Derive the expression for the input impedance of a non-inverting op-amp for ideal and practical cases?
   b) Draw and explain the function of all the basic building blocks of an op-amp? (8M+8M)

2. a) What is an instrumentation amplifier? Draw a system whose gain is controlled by an adjustable resistance?
   b) Design an adder circuit using an op-amp to get the output expression as $Vo = - (0.1V_1+V_2+10V_3)$? (10M+6M)

3. a) Discuss the advantages of active filters over passive filters?
   b) Design a band pass filter for $f_0 = 2$ kHz, $Q = 20$ and $A_v = 10$. Choose $C = 1\mu F$? (6M+10M)

4. a) With a circuit diagram explain the operation and derive the expression for time delay of a monostable multivibrator using IC 555 timer.
   b) Give the block diagram of IC 566 VCO and explain its operation? (8M+8M)

5. a) Draw the circuits and explain the operation of dual slope ADC?
   b) The basic step of a 9 bit DAC is 10.3 mV. If 000000000 represents 0V, what output is produced if the input is 101101101?? (8M+8M)

6. a) What is a logic family? Classify different types of logic families?
   b) Explain the three input NAND gate operation with TTL open collector output? (8M+8M)

7. a) Design a 32*1 MUX using 4*1 MUXs?
   b) Compare serial adder and parallel adder circuits? (10M+6M)

8. a) Distinguish between SRAM and DRAM?
   b) Design and Implement MOD-10 counters using J-K flip flops and explain its operation? (8M+8M)
~~~~~~~~~~~~~~~~~~~~~~~~~~

Code No: V0222 **R07** SET - 2

II B. Tech II Semester, Supplementary Examinations, April/May – 2013
LINEAR DIGITAL IC APPLICATIONS
(Electrical and Electronics Engineering)

Time: 3 hours Max. Marks: 80

Answer any **FIVE** Questions
All Questions carry **Equal** Marks
~~~~~~~~~~~~~~~~~~~~~~~~

1. Define following terms?
   i) Slew rate ii) Thermal drift iii) PSRR iv) Input bias current (4×4M=16M)

2. a) Draw a sample and hold circuit? Explain its operation and indicate its uses?
   b) What are the limitations of ordinary op-amp differentiator? How to eliminate their limitations. Explain. (10M+6M)

3. a) Design a wide band pass filter having f_l = 400 Hz, f_h = 2 kHz and pass band gain is 4. Find the value of Q of the filter?
   b) Draw and explain the triangular waveform generator? (8M+8M)

4. a) Discuss the operation of a FSK generator using 555 timer?
   b) Draw and explain the basic building blocks of PLL? (8M+8M)

5. a) Explain the operation of inverted R-2R ladder network?
   b) Explain the working of successive approximation type ADC? (8M+8M)

6. a) What is tristate logic? Explain its operation?
   b) Explain the operation of three input 'NOR' gate using CMOS technology. (6M+10M)

7. a) Design a 32*5 encoder using 8*3 encoders?
   b) Design a circuit that will convert gray code to binary code? (8M+8M)

8. a) Explain the operation of ROM architecture?
   b) Distinguish between RAM and ROM? (10M+6M)
~~~~~~~~~~~~~~~~~~~~~~~~

Code No: V0222 **R07** SET - 3

II B. Tech II Semester, Supplementary Examinations, April/May – 2013
LINEAR DIGITAL IC APPLICATIONS
(Electrical and Electronics Engineering)

Time: 3 hours Max. Marks: 80

Answer any **FIVE** Questions
All Questions carry **Equal** Marks
~~~~~~~~~~~~~~~~~~~~~~~~

1. a) List the advantages of integrated circuits over discrete component circuits?
   b) List the ideal characteristics of an ideal op-amp?
   c) Find the maximum frequency for a sine wave output voltage of 10V peak with an op-amp whose slew rate is 1V/μs? (5M +5M+6M)

2. a) Draw and explain the circuit of a voltage to current converter if the load is i) floating and ii) Grounded?
   b) Explain the operation of square wave generator using μA 741 IC and draw the capacitor and output voltage waveforms? (8M+8M)

3. a) Explain the operation of second order low pass filter with necessary equations?
   b) What is Wien bridge oscillator? How can you implement using μA 741 op-amp? (8M+8M)

4. a) Draw and explain the functional diagram of 555 timer?
   b) Calculate output frequency f_O, lock range Δfl and capture range Δfc of a 565 PLL if R_T = 10 KΩ, C_T = 0.01 μF and C = 10μF? (8M+8M)

5. a) Explain the operation of servo tracking ADC?
   b) What output voltage would be produced by DAC whose output range is 0 to 10 V and whose binary number is i) 10 ii) 0110 iii) 10111100 (6M+10M)

6. a) Draw the circuit diagram of CMOS inverter? Explain?
   b) Compare the TTL and CMOS logic families? (8M+8M)

7. a) Construct a full adder, using NOR gates only?
   b) Design a digital comparator that will compare three input? (8M+8M)

8. a) Explain with circuit diagram of right shift register?
   b) Explain the architecture of SRAM? (8M+8M)
~~~~~~~~~~~~~~~~~~~~~~~~

Code No: V0222 **R07** SET - 4

II B. Tech II Semester, Supplementary Examinations, April/May – 2013
LINEAR DIGITAL IC APPLICATIONS
(Electrical and Electronics Engineering)

Time: 3 hours Max. Marks: 80

Answer any **FIVE** Questions
All Questions carry **Equal** Marks
~~~~~~~~~~~~~~~~~~~~~~~~

1. a) What is frequency compensation? What is the need in op-amps?
   b) Explain the role of level translator in op-amps? (6M+10M)

2. a) How two analog voltages are multiplied using op-amps?
   b) Find the input resistance and feedback resistance in the lossy integrator so that the peak gain is 20 dB and the gain is 3 dB down from its peak when w = 10,000 rad/s. Choose C = 0.01μF? (6M+10M)

3. a) Design a fourth order Butterworth low pass filter having upper cut-off frequency 1 KHz?
   b) Implement narrow band pass filter using op-amps? (8M+8M)

4. a) Draw the circuit of a Schmitt trigger using 555 timer and explain?
   b) Derive the expression for lock-in-range and capture range in PLL. (8M+8M)

5. Define the following terms? (4×4M=16M)
   i) Linearity ii) Monotonicity iii) Accuracy iv) Settling time

6. a) Explain the three input NAND gate operation with TTL totem pole connection?
   b) Distinguish between transmission gate and logic gate? (10M+6M)

7. a) Design an octal to binary priority encoder?
   b) Implement 5 to 32 decoder using one 2 to 4 and four 3 to 8 decoders? (8M+8M)

8. a) Distinguish between synchronous and asynchronous counters?
   b) Draw and explain the architecture of DRAM? (8M+8M)
~~~~~~~~~~~~~~~~~~~~~~~~