Code No: R31026 **R10** **Set No: 1**

III B.Tech. I Semester Regular Examinations, November/December - 2012

LINEAR & DIGITAL IC APPLICATION

(Electrical and Electronics Engineering)

Time: 3 Hours **Max Marks: 75**

Answer any FIVE Questions

All Questions carry equal marks

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1. (a) Describe the classification of ICs in detail.
   (b) Discuss about dc analysis of Dual input balanced output amplifier.

2. (a) List out the AC characteristics of an op-amp and discuss about them.
   (b) With neat circuit diagrams explain the techniques used for minimizing offset voltage and offset current.

3 (a) Draw a neat circuit diagram of an integrator circuit. Explain its functioning with the input-output wave forms.Derive the output voltage V_0 of an integrator circuit.
   (b) Explain the principle of operation of a precision full wave rectifier with waveforms.

4 (a) Explain the operation of Schmitt trigger using 555 timer with its circuit diagram.
   (b)Draw the block diagram of a 565 PLL IC and explain its working. Derive the relation between the 'lock range' & 'capture range'.

5 (a) Explain the operation of an all pass filter with its circuit diagram. For an all pass filter, determine the phase shift Φ between the input and output at f=2 KHz.To obtain a positive phase shift 'Φ' what modifications are necessary in the circuit.
   (b)With the help of a neat circuit diagram and waveforms, explain the operation of a dual slope ADC. What are its special features.

6 (a) Explain the terms Multiplexing & Demultiplexing.
   (b) Implement full adder circuit using,
   i) Decoder, ii) Multiplexer
   (c) Design an 8421 to gray code converter.

7 (a) Compare synchronous & Asynchronous circuits
   (b) Design a Mod-6 synchronous counter using J-K flip flops.

8 (a) Explain the functional behavior of Static RAM cell
   (b) With the help of a circuit diagram, explain the read and write operations of a dynamic RAM cell.
   (c) Differentiate between static RAM and dynamic RAM.

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Code No: R31026 **R10** **Set No: 2**

III B.Tech. I Semester Regular Examinations, November/December - 2012

LINEAR & DIGITAL IC APPLICATION

(Electrical and Electronics Engineering)

Time: 3 Hours **Max Marks: 75**

Answer any FIVE Questions

All Questions carry equal marks

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1. (a) Explain the classification of ICs according to their method of fabrication.
   (b) Describe the AC analysis of differential amplifier to find the parameters A_d, A_c, R_i and R_o for dual input balanced output.

2. (a) Draw the basic block diagram of a general op-amp and explain the operation of each block.
   (b) List ideal characteristics of an op-amp and compare with that of a practical op-amp such as 741.

3. (a) Draw the circuit and explain the working of a logarithmic amplifier and derive the expression for its output.
   (b) Using a 741 op-amp design triangular /rectangular waveform generator to have a output frequency of 1 KHz, a triangular output amplitude of ±6V and a square wave output amplitude of approximately ±10V.

4. (a) Design and draw the circuit and explain the operation of a 555 Timer IC in Astable mode to get output wave form with 50% duty cycle.
   (b) Explain PLL with a block schematic and enlighten the terms: (i) free-running frequency f_0, (ii) lock range,(iii) capture range, and (iv) pull-in time, pertaining to PLL.

5. (a) Show how a band stop filter circuit can be constructed by the use of low pass and high pass filters. Sketch the expected frequency response and briefly explain.
   (b) Draw the circuit of weighted resistor DAC and derive expression for output analog voltage Vo.

6. (a) Describe the terms decoder & de-multiplexer. How can you convert a decoder into a de-multiplexer?
   (b) Design a 4 bit BCD to Excess- 3 code converter

7. Design a 4 bit universal shift register which can be used as a parallel in- parallel out register, serial in serial out register, serial in - parallel out and parallel in serial out register with a shift option to wards left or right. Explain each of the behavior with timing waveform.

8. (a)Specify the size of a ROM (number of words and numbers bits per word) that will accommodate the truth table of a BCD to seven segment decoder with an enable input.
   (b) Write a brief note on "programmable logic devices".

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Code No: R31026 **R10** **Set No: 3**

III B.Tech. I Semester Regular Examinations, November/December - 2012

LINEAR & DIGITAL IC APPLICATION

(Electrical and Electronics Engineering)

Time: 3 Hours **Max Marks: 75**

Answer any FIVE Questions

All Questions carry equal marks

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1. (a) Discuss the properties of dual input unbalanced output, single ended input differential amplifier.
   (b) Write short notes on "Level Translator".

2. (a) Define and explain the following op-amp parameters.
   (i) Input offset voltage; (ii); CMRR; (iii) PSRR; (iv) Slew Rate
   (b) Explain frequency compensation techniques used in op-amps.

3. (a) Draw the circuit and discuss the working of an instrumentation amplifier? What are its important features? Derive an expression for its output.
   (b) Explain with a neat circuit diagram the working of voltage to current converter with floating load.

4. (a) Draw the circuit diagram and explain the operation of Monostable multivibrator using 555 timer with relevant waveforms. Derive the expression for the output pulse width.
   (b) Give the functional block diagram of VCO NE566 and explain its working.

5. (a) Explain the operation of R-2R-ladder type DAC. Write briefly on performance specifications of digital to analog converter.
   (b) Design a narrow bandpass filter with butterworth response for the following specifications f_0 = 10 kHz, Q = 10 and passband gain $\geq$ 10.

6. (a) What is a demultiplexer? Mention the differences between DMUX and MUX. Implement the function f = Σm (0, 1, 4, 5, 7) using 8 to 1 multiplexer.
   (b) Design a 4 bit BCD to Excess- 3 code converter using Binary Parallel Adder (BPA). What is the drawback in BPA and how can it be rectified.

7. (a) Realize a master-slave JK Flip-Flop using NAND gates and explain its operation with the help of its truth table. Mention its merits over edge- triggered JK Flip-Flop.
   (b) Design a modulo-100 counter using two 74×163 binary counters?

8. (a) How does the architecture of PLA different from PROM? Explain.
   (b) Explain with suitable diagram the internal structure of a DRAM cell.

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Code No: R31026 **R10** **Set No: 4**

III B.Tech. I Semester Regular Examinations, November/December - 2012

LINEAR & DIGITAL IC APPLICATION

(Electrical and Electronics Engineering)

Time: 3 Hours **Max Marks: 75**

Answer any FIVE Questions

All Questions carry equal marks

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1. (a) Briefly explain the difference between digital and linear ICs.
   (b) List different types of linear IC packages.
   (c) What is a level translator circuit? Why it is used with the cascaded differential amplifier in op-amps?

2. (a) Explain the significance of the following OPAMP parameters
   (i) CMRR (ii) PSRR and (iii) Slew rate
   What is the effect of these parameters on the performance of operational amplifier.
   (b) Draw and explain the working of an op amp with offset-voltage compensating network.

3. (a) Design a differentiator to differentiate an input signal that varies in frequency from 10Hz to about 1K Hz. Draw its output waveform if sin $2\pi\times1000t$ signal is applied.
   (b) Define the terms Upper and Lower Points of a Schmitt trigger. What is the significance of the two parameters? Explain the operation of a Schmitt trigger circuit using comparator.

4. (a) Draw the functional diagram of a 555 timer IC and explain the function of each internal block to obtain Astable multivibrator operation
   (b) What is the purpose of low pass filter in a phase locked loop? Describe different types of low pass filters used in PLL.

5. (a) Design & draw the circuit of a notch filter for f_N=8 KHz and Q=10. Choose C=500 pF.
   (b) Draw the schematic diagram of Successive Approximation type analog to digital converter and explain the operation.

6. (a) Explain how a 4 to 16 line decoder can be built using 2 to 4 line decoder.
   (b) Draw and explain the working of 4 bit adder – subtractor circuit

7. (a) Explain the working of JK flip-flop. What is race around condition? How is it overcome? Explain these concepts with relevant timing diagrams.
   (b)Sketch the block diagram for a Johnson (twisted-ring) counter & explain its operation. Draw the output waveform from each flip- flop of a three stage unit. By what number N does this system divide.

8. (a) How does the architecture of PLA different from PROM? Differentiate between PLA, ROM and PAL
   (b) Sketch the circuit of a 6 –MOSFET static RAM cell and explain its operation.

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