Code No: V0421 **R07** SET - 1

II B. Tech II Semester, Supplementary Examinations, April/May – 2013
PULSE AND DIGITAL CIRCUITS
(Com. to ECE, ECC, BME)

Time: 3 hours Max. Marks: 80

Answer any **FIVE** Questions
All Questions carry **Equal** Marks
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1. a) A Symmetrical square wave of peak-to-peak amplitude 'V' and frequency 'f 'is applied to a RC High pass circuit. Show that the fractional tilt is given by $P = \pi f_1/f$. Where f_1 is the lower 3dB frequency of RC High pass circuit.
   b) RC Low pass circuit with R = 40 kilo-ohms, C = 0.2μf is given a square wave input of 20V peak and 10msec period. What will be the amplitude of settled output voltage wave form.

2. a) Explain how a sine wave may be converted into a square wave using a clipping circuit.
   b) With help of a neat circuit diagram and waveforms explain the working of a positive clamping circuit.

3. a) Explain in detail about (i) Diode forward recovery time (ii) Diode reverse recovery time.
   b) With a neat circuit diagram and waveforms explain the operation of transistor switch.

4. a) With a neat circuit diagram and relevant waveforms explain the operation of a Schmitt trigger using BJTs.
   b) Design a collector coupled monostable multivibrator with the following specifications: V_{cc} = +12V, V_{bb} = -6V, h_{FEmin} = 20, V_{EBO} = 5V, I_c = 20mA.
   Transistors are of silicon npn type. Output pulse width = 200μsec.

5. a) Derive the expressions for Slope error, Transmission error and displacement error. Establish the inter-relationship among them.
   b) Draw the circuit diagram of Bootstrap time base generator and explain the Operation with the help of waveforms.

6. a) With the help of a neat circuit diagram and waveforms, explain the synchronization of a sweep generator with pulse signals.
   b) Explain the use of a monostable relaxation device as divider.

7. a) With the help of a neat circuit diagram and waveforms, explain the operation of unidirectional diode sampling gate.
   b) With the help of a neat circuit diagram and waveforms, explain the operation of bidirectional sampling gate using transistor.

8. a) With the help of neat circuit diagram and truth table explain
   i) DL AND gate ii) RTL AND gate.
   b) With the help of neat circuit diagram and truth table explain
   i) DTL NAND gate ii) RTL NAND gate.

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Code No: V0421 **R07** SET - 2

II B. Tech II Semester, Supplementary Examinations, April/May – 2013
PULSE AND DIGITAL CIRCUITS
(Com. to ECE, ECC, BME)

Time: 3 hours Max. Marks: 80

Answer any **FIVE** Questions
All Questions carry **Equal** Marks
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1. a) Derive the relation between rise time and upper cut-off frequency of RC low pass circuit.
   b) RC high pass circuit with time constant RC is 1 ms given a 1 kHz symmetrical square wave of +/- 10V. Calculate and plot the settled output voltage wave form.

2. a) Design and draw a diode clipper circuit to clip the given input voltage of 10 sinωt at +3Vand -5V level. Sketch the waveforms neatly.
   b) State and prove clamping circuit theorem.

3. a) Explain in detail about storage and transition times relating to diode switching times.
   b) Discuss in detail about transistor switching times.

4. a) Derive the expressions for UTP and LTP of a Schmitt trigger.
   b) Show an astable multivibrator can be used as a voltage to frequency converter.

5. a) Explain in detail about basic principles of Miller and bootstrap time-base generators.
   b) With the help of a neat circuit diagram, explain the working of a simple current sweep.

6. a) With the help of a neat circuit diagram and waveforms, explain the frequency division with respect to a sweep circuit.
   b) Explain synchronization of sweep circuit with symmetrical signals.

7. a) With the help of a neat circuit diagram and waveforms, explain the operation of unidirectional diode sampling gate to accommodate more than one input signal.
   b) Explain in detail about one application of sampling gates.

8. a) With the help of neat circuit diagram and truth table explain
      i) DL OR gate ii) RTL OR gate.
   b) With the help of neat circuit diagram and truth table explain
      i) DTL NOR gate ii) RTL NOR gate.
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Code No: V0421 **R07** SET - 3

II B. Tech II Semester, Supplementary Examinations, April/May – 2013
PULSE AND DIGITAL CIRCUITS
(Com. to ECE, ECC, BME)

Time: 3 hours Max. Marks: 80

Answer any **FIVE** Questions
All Questions carry **Equal** Marks
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1. a) Derive the condition for perfect compensation of an attenuator.
   b) RC Low pass circuit with R = 5 kilo-ohms, C = 0.1μf is given a symmetrical square wave of amplitude +/- 5Vand frequency 2 kHz. What will be the amplitude of settled output voltage wave form?

2. a) With help of a neat circuit diagram and waveforms explain the operation of a transistor clipper.
   b) With help of a neat circuit diagram and waveforms explain the operation of a Simple diode comparator.

3. a) Explain in detail about piece-wise linear diode characteristics.
   b) Discuss in detail about breakdown voltages of a transistor.

4. a) With the help of a neat circuit diagram, explain the operation of a emitter coupled monostable multivibrator.
   b) Derive an expression for frequency of oscillation of a astable multivibrator.

5. a) With the help of a neat circuit diagram, explain the working of a transistor miller sweep.
   b) With the help of a neat circuit diagram, explain the working of a transistor current time-base generator.

6. a) With the help of a neat circuit diagram and waveforms, explain the frequency division By astable blocking oscillator.
   b) With the help of a neat waveforms, explain sine wave frequency division with a sweep circuit.

7. a) With the help of a neat circuit diagram and waveforms, explain the operation of bidirectional diode sampling gate.
   b) Explain in detail about one application of sampling gates.

8. a) With the help of neat circuit diagram and truth table explain
      i) DL AND gate ii) RTL AND gate.
   b) With the help of neat circuit diagram and truth table explain
      i) DTL NOR gate ii) RTL NOR gate.
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Code No: V0421 **R07** SET - 4

II B. Tech II Semester, Supplementary Examinations, April/May – 2013
PULSE AND DIGITAL CIRCUITS
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Time: 3 hours Max. Marks: 80

Answer any **FIVE** Questions
All Questions carry **Equal** Marks
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1. a) Derive the expression for the percentage tilt of the output of high pass circuit with large time constant excited by a symmetrical square wave with zero average value.
   b) 1 kHz square wave output from an amplifier has rise time t_r = 350ns and tilt = 5%. Determine the upper and lower 3-db frequencies.

2. a) With help of a neat circuit diagram and waveforms explain the operation of an Emitter coupled clipper.
   b) With help of a neat circuit diagram and waveforms explain the working of a negative clamping circuit.

3. a) Explain the operation of transistor switch in saturation.
   b) For a common emitter amplifier, V_{cc} = 15V, R_c = 1.5kΩ and I_B = 0.3 mA.
      i) Determine the value of $h_{FE(mim)}$ for saturation to occur.
      ii) If R_c is changed to 500Ω will the transistor be saturated.

4. a) Derive an expression for gate width of a monostable multivibrator.
   b) With the help of a neat circuit diagram, explain the operation of a astable multivibrator.

5. a) Explain briefly about different methods of generating time-base waveform.
   b) Discuss in detail about correction of linearity through the adjustment of driving waveform for a current time-base waveform.

6. a) With the help of a neat circuit diagram and waveforms, explain the frequency division By astable multivibrator
   b) Explain in detail about pulse synchronization of monostable circuits.

7. a) With the help of a neat circuit diagram and waveforms, explain the operation of Four diode sampling gate.
   b) With the help of a neat circuit diagram and waveforms, explain the operation of Six diode sampling gate.

8. a) With the help of neat circuit diagram and truth table explain
      i) DL OR gate ii) RTL OR gate.
   b) With the help of neat circuit diagram and truth table explain
      i) DTL NAND gate ii)RTL NAND gate.

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