Code: R7210203

R07

B.Tech II Year I Semester (R07) Supplementary Examinations, May 2013

PULSE AND DIGITAL CIRCUITS

(Common to EEE and EIE)

Time: 3 hours Max. Marks: 80

Answer any FIVE questions

All questions carry equal marks

*****

1 (a) Derive an expression for the rise time of the output of a low pass circuit excited by a step input.

(b) A pulse with a rise time $t_r = 500\ ns$ and a fall time $t_f = 1\ \mu s$. Pulse amplitude 12 V and pulse width $10\ \mu s$ is applied to a differentiating circuit with $C = 200\ PF$ and $R = 470\ \Omega$. Determine the amplitude of the differentiated output.

2 (a) With the help of a neat circuit diagram, explain the working of a two level diode clipper.

(b) Discuss the effect of diode characteristics on clamping voltages.

3 (a) Explain the working of transistor as an inverter with the help of circuit diagram and waveforms.

(b) Explain various transistor switching times.

4 (a) With the help of a neat circuit and waveforms, explain the working of an astable blocking oscillator.

(b) Show that gate width of a collector coupled monostable multi-vibrator is 0.69 RC.

5 (a) Write notes on sweep generators.

(b) Explain the principle of miller boot strapping circuit.

(c) Give the applications of time base generators.

6 (a) What is relaxation oscillator? Explain pulse synchronization of relaxation oscillator with necessary diagrams.

(b) What is synchronization with frequency division? Give an example of synchronization with frequency division.

7 (a) With the help of a neat diagram, explain the working of two diode sampling gate.

(b) Write the advantages and disadvantages of unidirectional diode gate.

8 (a) Give applications of logic gates. Define positive and negative logic systems.

(b) Construct a AND gate from a basic DTL gate and explain its circuit diagram.

*****