Code: 9A04404

1

B.Tech II Year II Semester (R09) Regular & Supplementary Examinations, April/May 2013
PULSE AND DIGITAL CIRCUITS
(Common to EIE, E.Con.E, ECE, ECC and MCT)

Time: 3 hours   Max Marks: 70

Answer any FIVE questions
All questions carry equal marks
*****

1 (a) Derive the conditions necessary for good integrator.
   (b) A square wave whose peak to peak amplitude is 1 V extends ± 0.5 V with respect to ground. The duration of the positive section is 0.1 sec and of the negative section is 0.2 sec. If this wave form is impressed on RC high pass circuits whose time constant is 0.2 sec? What are the steady state maximum and minimum values of the output waveform?

2 (a) Explain transfer characteristics of the emitter coupled clipper and derive the necessary equations.
   (b) Draw the basic circuit diagram of positive peak clamper circuit and explain its operation.

3 (a) Explain with relevant diagram the various transistor switching times.
   (b) Explain the storage and transition times of the diode as a switch.

4 (a) Explain how a Schmitt trigger can be used as a comparator and as a squaring circuit.
   (b) What do you understand by hysteresis? What is hysteresis voltage? Explain how hysteresis can be eliminated in a Schmitt trigger.

5 (a) Draw the circuit of RC ramp generator using bipolar transistor constant current circuit.
   (b) Sketch typical input and output waveforms and briefly explain the circuit operation.

6 (a) What are different factors that cause phase delay?
   (b) What is 6 to 1 frequency division? Explain.

7 (a) What is synchronization?
   (b) What is the condition to be met for pulse synchronization?

8 (a) Explain 3 load configuration of a MOS gate.
   (b) Explain why CMOS and TTL gates could not be interfaced directly even though both operate at 5 V supply.

*****

Code: 9A04404

| **2** |

B.Tech II Year II Semester (R09) Regular & Supplementary Examinations, April/May 2013

PULSE AND DIGITAL CIRCUITS

(Common to EIE, E.Con.E, ECE, ECC and MCT)

Time: 3 hours   Max Marks: 70

Answer any FIVE questions
All questions carry equal marks
*****

1   Write short note on the following:
- (a)   Attenuators.
- (b)   RC Double differentiator.
- (c)   RLC ringing circuit.

2 (a)   Explain the response of the clamping circuit when a square wave input is applied under steady state conditions.
- (b)   Explain the effect of diode characteristics on clamping voltage.

3 (a)   Explain how transistor will act as switch.
- (b)   Discuss about unsymmetrical triggering of multivibrator.

4   A fixed bias bistable has the following circuit parameters R_C = 1 kΩ, R_1 = 3.9 kΩ, V_{CC} = + 9V and V_{BB} = - 9 V. Assume for transistor V_{CEsat} = 0 V, V_{BEsat} = 0.6 V and $V_{BE(cutoff)}$ = 0 V. Analyze the binary, and find the stable state voltages and currents. What is the minimum value of h_{FE} to satisfy the ON-OFF condition? Draw the circuit diagram and corresponding waveforms at both collections and bases.

5 (a)   Explain about transistor television sweep circuit.
- (b)   List applications of voltage and current sweep generators.

6 (a)   Explain the operation of series and shunt FET sampling gates.
- (b)   What are the advantages of FET sampling gates over transistor sampling gates?

7 (a)   Explain how monostable multi is used as frequency divider.
- (b)   Draw and explain the block diagram of frequency divider without phase jitter.

8 (a)   Explain and draw the sinking sourcing characteristics of TTL.
- (b)   Draw a positive NAND gate with diodes and a transistor (DTL) and explain its operation.

*****

Code: 9A04404

<div style="border:1px solid black; display:inline-block;">**3**</div>

B.Tech II Year II Semester (R09) Regular & Supplementary Examinations, April/May 2013
PULSE AND DIGITAL CIRCUITS
(Common to EIE, E.Con.E, ECE, ECC and MCT)

Time: 3 hours   Max Marks: 70

Answer any FIVE questions
All questions carry equal marks
*****

1 (a) A 10 Hz symmetrical square wave whose peak-to-peak amplitude is 2 V is impressed on a high-pass circuit whose lower 3-dB frequency is 5 Hz. Calculate and sketch the output waveform.
   (b) What is the peak to peak output amplitude of the above wave form?

2   Draw the circuit diagram of emitter coupled clipper. Draw its transfer characteristics indicating all intercepts, slopes and voltage levels derive the necessary equations.

3 (a) Explain with relevant diagrams the various transistor switching times.
   (b) Explain the tests that can be performed for listing of a transistor for saturation.
   (c) Give the design considerations of a transistor switch.

4   What is a monostable multivibrator? Explain with the help of a neat circuit diagram the principle of operation of a monostable multivibrator, and derive an expression for pulse width. Draw the wave forms at collector and bases of both transistors.

5 (a) Explain about performance deviations of time base generators.
   (b) What are the methods of generating time base waveforms?

6 (a) Define sampling gate and explain.
   (b) With neat diagram explain the principle of operation of four diode bidirectional sampling gate.

7   Distinguish between astable frequency division and monostable frequency division with neat wave forms and analysis along with mathematical derivations.

8   Distinguish between static and dynamic power4 dissipation of a CMOS circuit. Derive the expression for dynamic power dissipation.

*****

Code: 9A04404

4

B.Tech II Year II Semester (R09) Regular & Supplementary Examinations, April/May 2013
PULSE AND DIGITAL CIRCUITS
(Common to EIE, E.Con.E, ECE, ECC and MCT)

Time: 3 hours   Max Marks: 70

Answer any FIVE questions
All questions carry equal marks
*****

1 (a)   Derive the output and draw the response of high pass RC circuit for:
        (i) Step input.   (ii) Square input.
  (b)   What is an attenuator? Explain the under and over compensation in attenuator.

2 (a)   Give the circuits of series clipper circuits and explain their operation with the help of transfer characteristics.
  (b)   Draw the circuit diagram of emitter coupled clipper. Draw its transfer characteristics indicating all intercepts, slopes and voltage levels derive the necessary equations.

3 (a)   Explain how diode will act as switch.
  (b)   Discuss the applications of Schmitt trigger.

4 (a)   Discuss the different methods of triggering a flip-flop. Explain the role of commutating capacitors in a binary circuit.
  (b)   Draw the circuit diagram of a fixed bias binary with speed up capacitors.

5 (a)   Compare boot strap time base circuit and miller time base circuit.
  (b)   Compare voltage time base circuit and current time base circuit.

6 (a)   What is pedestal? How it affects the output of a sampling gate?
  (b)   Describe the operation of chopper amplifier.

7 (a)   With the help of a circuit diagram and wave forms explain the frequency division by an astable multivibrator?
  (b)   Explain the terms synchronization and frequency division of a sweep generator.

8 (a)   Design OR and NAND by using CMOS.
  (b)   What are the advantages and disadvantages of open collector outputs?

*****