

Code No: R09220204

R09**Set No. 2**

**II B.Tech II Semester Examinations, APRIL 2011
SWITCHING THEORY AND LOGIC DESIGN**

Common to Bio-Medical Engineering, Electronics And Telematics,
Electronics And Communication Engineering, Electrical And Electronics
Engineering

Time: 3 hours

Max Marks: 75

Answer any FIVE Questions
All Questions carry equal marks

1. Construct a combinational logic circuit which converts a decimal number into an equivalent Excess -3 number. Implement the same using

(a) Multiplexer

(b) Decoder

[15]

2. (a) i. Convert $(1596.675)_{10}$ to hexadecimal
ii. Convert $(11110.1011)_2$ to decimal
iii. Convert $(10110001.01101001)_2$ to octal
iv. Convert $(235.0657)_8$ to Binary

(b) Obtain the 1's complement and 2's complement of the binary numbers

i. 1011011

ii. 0110101

iii. 10110

iv. 00110

[8+7]

3. Construct the compatibility graph and obtain the minimal cover table for the sequential machine described by the state table given. [15]

PS	NS,Z	
	I=0	I=1
1	2,0	3,1
2	1,0	1,1
3	4,1	4,1
4	3,1	6,0
5	1,0	1,1
6	7,0	6,0
7	4,1	4,1

4. (a) Write the conversion procedures of the flip flops. Convert T flip flop to JK flip flop.

(b) Convert SR flip flop to T flip flop.

[8+7]

5. Map the following function and simplify using K-Map

$$(a) F = (A+B+C)(A+B'+C)(A+B'+C')(A'+B+C)$$

Code No: R09220204

R09**Set No. 2**

$$(b) F = (A'BC'D' + A'BC'D + AB'CD + AB'CD' + ABCD + A'B'C'D') \quad [15]$$

6. Write short notes on Integrated circuits. Classify the ICs based on the levels of integration. Discuss on PLDS. What are the different types of programmable devices? [15]

7. A sequential circuit has three D flip flops, A, B, C and one input x. The minterms of the D flip flops are given below. Construct the State table and Draw an ASM chart.

$$D_A(X,A,B,C) = \Sigma (0,3,4,7,9,10,13,14)$$

$$D_B(X,A,B,C) = \Sigma (4,5,6,7,12,13,14,15)$$

$$D_C(X,A,B,C) = \Sigma (2,3,6,7,10,11,14,15) \quad [15]$$

8. (a) Write short notes on Universal gates

(b) Implement $Y = AB' + CD + (A'B + C'D')$ using NAND gates

(c) Verify the following Boolean algebraic expression. Justify each step with a reference to a theorem or postulate.

$$(AB + C + D)(C' + D)(C' + D + E) = ABC' + D \quad [4+4+7]$$

Code No: R09220204

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1. (a) Draw an ASM chart to convert D-Flip flop to T flip flop.
(b) Give the procedure to design a data processing unit and a control unit. [8+7]
2. (a) Define the following with an example
 - i. Canonical form
 - ii. Standard form
 - iii. Minterm
 - iv. Maxterm
- (b) Draw the truth table and write Boolean expression for the following:
 - i. F is a 1 only if X is a 1 and Y is a 1 or if X is 0 and Y is a 0.
 - ii. G is a 0 if any of the three variables X, Y and Z are 1s. G is a 1 for all other conditions. [8+7]
3. Realize the function $F = (A'+C)(AB'+C)(C+D')$ in
 - (a) Decoder
 - (b) Multiplexer

Explain in detail the procedure to implement the Boolean functions in decoder and multiplexer. [15]

4. (a) Write short notes on :
 - i. State transition function.
 - ii. Finite State model.
 - iii. Terminal state
 - iv. Strongly connected machine
- (b) Discuss on the capabilities and limitations of finite state machines. [8+7]
5. (a) Use 1's complement arithmetic to subtract
 - i. $(54)_{10}$ from $(231)_{10}$
 - ii. $(-27)_{10} - (87)_{10}$
- (b) Determine the largest and smallest. Hexadecimal numbers that can be used in a 16-bit digital system. [8+7]

Code No: R09220204

R09

Set No. 4

6. Implement the following functions using PAL and PLA
F1 = $\Sigma m(2,3,4,7,8,11)$
F2 = $\Sigma m(1,3,5,7,9,11,13,15)$ [15]
7. (a) Design a 4-bit Bidirectional Shift Register.
(b) Convert D flip flop to T flip flop. [8+7]
8. Design a combinational logic circuit with 4 inputs A, B, C, D. The output Y goes HIGH if and only if A and C inputs go HIGH. Draw the Truth table. Minimize the Boolean function using K-map. Draw the circuit diagram. [15]

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Code No: R09220204

R09**Set No. 1**

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1. Simplify the following expressions using K-map

- (a) $x'(y'+z)$
- (b) $x'+y'+xyz'$
- (c) $xy+wxyz'+x'y$
- (d) $w'x'+x'y'+w'z'+yz$

[15]

2. Determine a minimal state table equivalent to the state table given below. [15]

PS	NS,Z	
	J1	J2
1	2,0	4,1
2	7,0	1,0
3	4,0	2,1
4	7,0	1,0
5	4,0	1,1
6	5,1	6,1
7	4,1	4,1

3. (a) Differentiate Hexadecimal codes and Alpha numeric codes.

(b) Write Gray codes for the following decimal numbers:

- i. 1000
- ii. 724
- iii. 83
- iv. 37

[7+8]

4. (a) A Digital system is quite often defined by registers it contains and operations that are executed on the data stored in them. Give examples of symbolic notation of register operation and its descriptions.

(b) Draw an ASM diagram and explain in detail the conditional box. [8+7]

5. (a) Give a detailed comparison between combinational logic circuits and sequential logic circuits.

(b) Design a basic flip flop and explain its operation. [8+7]

Code No: R09220204

R09

Set No. 1

6. Tabulate the PLA programming table for the four Boolean functions. Minimize the following.
- (a) $F1(A, B, C) = \Sigma m(1, 2, 5, 6)$
 - (b) $F2(A, B, C) = \Sigma m(0, 1, 4, 7)$
 - (c) $F3(A, B, C) = \Sigma m(2, 6, 8)$
 - (d) $F4(A, B, C) = \Sigma m(1, 2, 3, 5, 7)$ [15]
7. Design a Logic circuit which accepts two 5 bit binary numbers. The circuit should perform binary addition when the carry in is 0 and should perform binary subtraction using 2's complement addition when the input carry is 1. [15]
8. Draw the logic circuits using AND, OR, NOT elements to represent the following:
- (a) $AB' + A'B$
 - (b) $((AB)'(CD)')'$
 - (c) $((A+B)(C+D))E + FG$
 - (d) $AB + (AB)' + A'BC$

Implement the above functions using only NAND gates and only NOR gates [15]

Code No: R09220204

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1. Convert the following Mealy machine into a corresponding Moore machine. [15]

PS	NS,Z	
	X=0	X=1
A	C,0	B,0
B	A,1	D,0
C	B,1	A,1
D	D,1	C,0

2. (a) Demonstrate by means of truth tables the validity of the following theorems of Boolean algebra.

- i. Commutative laws
- ii. Demorgan's theorems for 4 variables.

- (b) Prove the following:

i. $XYZ + XYZ' + XY'Z + X'Y'Z + X'YZ' = Y'Z + XY + X'YZ'$

ii. $XY' + Y'Z = XY'Z + XY'Z' + X'Y'Z$ [8+7]

3. Draw the block diagram of the 3 to 8 decoder. Draw the circuit diagram of the decoder and explain the operation of the decoder.

- (a) If the input 3 bit code is 110, then which decoder output will be HIGH?
- (b) If the output of the decoder D3 is HIGH, what is the input code of the decoder? [15]

4. (a) Explain the complement representation of negative numbers with examples

- (b) Obtain the 1's complement and 2's complement of the binary numbers

i. 1010111

ii. 0111001

iii. 1001

iv. 00010

[4+11]

5. Implement the function of converting a Binary number to a BCD number in a ROM. Write the size of ROM required implementing this function. Give the ROM truth table. Give the internal connections for the function. [15]

Code No: R09220204

R09

Set No. 3

6. (a) Draw an ASM chart for designing a circuit which is used to count the number of bits in a register that have a value 1.
(b) Discuss the procedure to implement an ASM chart using Multiplexer. [8+7]
7. Define State table. Draw state table for a 4 bit synchronous UP/DOWN counter. Design UP/DOWN synchronous counters. [15]
8. (a) List down the factors involved in a digital circuit design. Specify the various criteria to determine minimal cost.
(b) Compare the Minimization procedure using Boolean Postulates and K-map. [8+7]

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