CODE NO: R09220403 | R09 | SET No - 1

II B.TECH - II SEMESTER EXAMINATIONS, APRIL/MAY, 2011
PULSE AND DIGITAL CIRCUITS
(COMMON TO ELECTRONICS AND COMMUNICATION ENGINEERING, ELECTRONICS AND TELEMATICS)

Time: 3hours **Max. Marks: 75**

Answer any FIVE questions
All Questions Carry Equal Marks

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1.a) The output of a high pass RC circuit for a symmetrical square wave input is shown in Figure.1. Derive the expression for percentage tilt in the output.

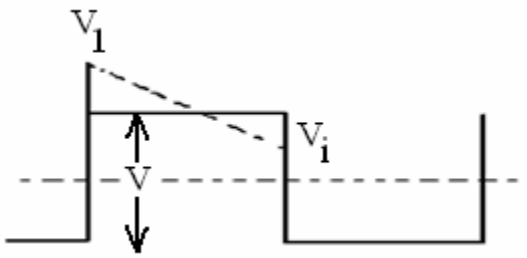

Figure.1

b) An oscilloscope displays a 5Hz square wave with 6% tilt. The signal input has no tilt and is coupled to the oscilloscope via a 4.7μF capacitor. Calculate the input resistance of the oscilloscope. [10+5]

2.a) Draw the circuit diagram of an Emitter-Coupled clipping circuit. Explain its operation with its transfer characteristic and necessary expressions

b) State and prove clamping circuit theorem. [8+7]

3.a) A silicon transistor has h_{FE} = 75, I_{CO} = 0.1μA and cut-in voltage V_γ = 0.5V. The parameter "n" of avalanche multiplication is 4 and BV_{CBO} = 50V.
i) Calculate BV_{CEO}
ii) Calculate BV_{CER} if R_B = 1.M Ω
iii) Calculate BV_{CEX} assuming V_{BB} = 10V and R_B = 10K.

b) Write about diode switching times. [10+5]

4.a) What are transpose capacitors? Explain how the commutating capacitors will increase the speed of a fixed-bias binary.

b) For the circuit shown in figure.4, Vcc = 18V, V_{BB} = 6V, V = 6V, Rc = 1.5K, R_1= 5K, R_2 = 25K and h_{FE}(min) of each transistor is 40. Neglect the drop across the forward biased junctions. Indicate all the circuit voltages in the quiescent state and indicate also the voltages immediately after a 5V positive step is applied. [5+10]

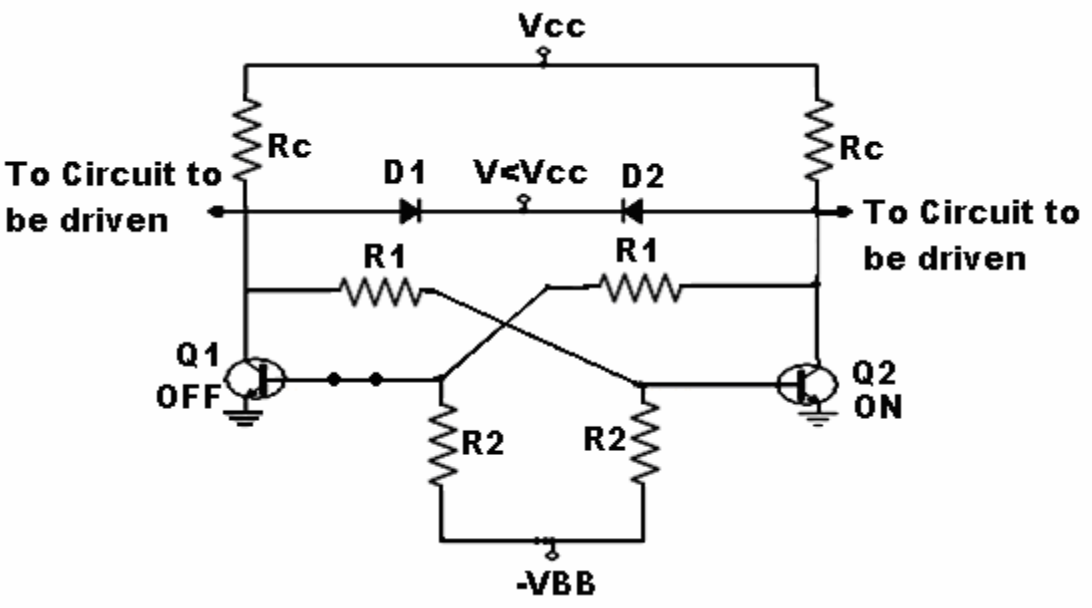

Figure.4

5.a) Draw the circuit of a Boot strap sweep generator and explain its operation. Derive an expression for its sweep time.

b) Explain with a circuit the working of a UJT sweep circuit and obtain the expressions for the intrinsic standoff ratio (η). [8+7]

6.a) Illustrate with neat circuit diagram, the operation of unidirectional sampling gate for multiple inputs.

b) Explain with circuit diagram the operation of a two input sampling gate which does not have any loading effect on control signal. [7+8]

7.a) With neat waveforms explain sine wave synchronization and compare it with pulse synchronization.

b) The relaxation oscillator when running freely, generates an output sweep amplitude of 100V and frequency 1kHz. Synchronizing pulses are applied such that at each pulse the breakdown voltage is lowered by 20V. Over what frequency range the synchronizing pulse frequency may be varied if 1:1 synchronization is to result? [8+7]

8.a) Realize two-input AND & OR gates using diodes and explain their operation with the help of truth-tables.

b) Realize a three-input NOR gate using Resistor Transistor Logic and explain its operation with the help of truth-table. [8+7]

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1.a) Prove that an RC circuit behaves as a reasonably good integrator if RC > 15T, Where T is the period of an input '$E_m \sin \omega t$'.

b) What is the ratio of the rise time of the three sections in cascade to the rise-time of Single section of low pass RC circuit? [8+7]

2.a) A square wave input of period T = 1000 μ sec, Vpeak = 10V and Duty cycle = 0.2 is applied to the circuit shown in figure.2. Given, R_S = 100Ω, C = 1μF, R = 10K & Diode forward resistance, R_f = 100Ω.
i) Sketch the output waveform with voltage levels at steady state.
ii) Forward and reverse direction tilt
iii) A_f / A_r

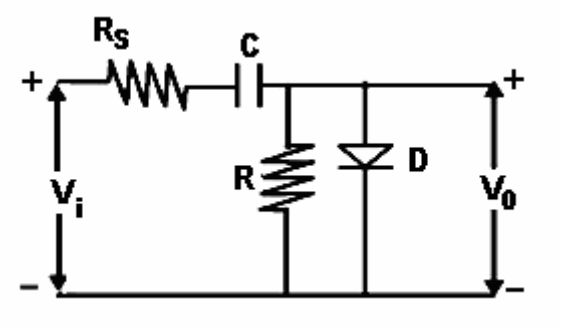

figure.2

b) Write a short note on voltage comparators. [12+3]

3.a) Explain the terms pertaining to transistor switching characteristics.
i) Rise time. ii) Delay time. iii) Turn-ON time.
iv) Storage time. v) Fall time. vi) Turn-OFF time.

b) Calculate the maximum operating frequency of a diode with storage time of 1ns and transition time of 8ns. [12+3]

4.a) What do you mean by collector catching diodes? Explain the need of these diodes in a bistable multivibrator.

b) For the given circuit shown in figure. 4, find UTP & LTP. What is this circuit called? Data given h_{fe}(min) = 40, V_{CE}(sat) = 0.1 V, V_{BE}(sat)=0.7 V, V_γ = 0.5V, V_{BE}(active) = 0.6V.

[5+10]

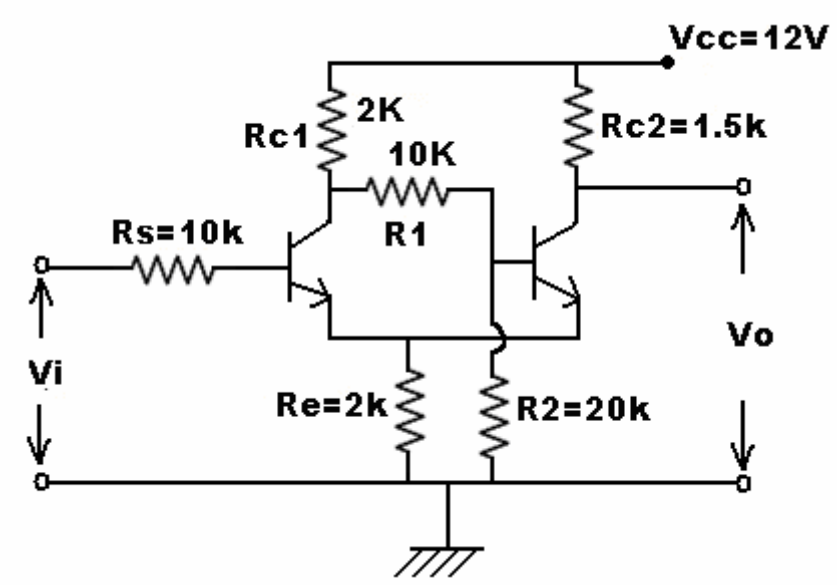

figure.4

5.a) Define the three errors that occur in a sweep circuit and obtain an expression for these errors for an exponential sweep circuit.

b) In the UJT sweep circuit, V_{BB} = 20V, V_{yy} = 50V, R = 5k, C = 0.01 micro F. UJT has η= 0.5. Calculate
i) Amplitude of sweep signal
ii) Slope and displacement errors and
iii) Estimated recovery time. [8+7]

6.a) With the help of a neat diagram, explain the working of two-diode sampling gate.

b) Derive expressions for gain and minimum control voltages of a bi-directional two- diode sampling gate. [7+8]

7.a) Explain how monostable multivibrator is used as frequency divider?

b) Write short notes on
i) Phase delay
ii) Phase jitters [7+8]

8.a) What is logical noise in a diode AND gate? Explain how it can be reduced by connecting a clamping diode in the circuit?

b) Realize NAND & NOR gates using CMOS Logic and explain their operation with the help of truth-tables. [7+8]

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Answer any FIVE questions
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1.a) What are the drawbacks of uncompensated attenuators? Prove that the condition to prevent input signal from distortion is $R_1C_1 = R_2C_2$, in an adequately compensated attenuator.

b) An RC differentiator circuit is driven from a 500Hz symmetrical square wave of 10V Peak-to peak. Calculate the output voltage levels under steady state if RC = 1msec.[10+5]

2.a) Draw the basic circuit diagram of negative peak clamper and explain its operation.

b) For the circuit shown in figure.2, an input voltage V_i linearly varies from 0 to 150V is applied. Sketch the output voltage V_O and transfer characteristics. Assume ideal diodes. [5+10]

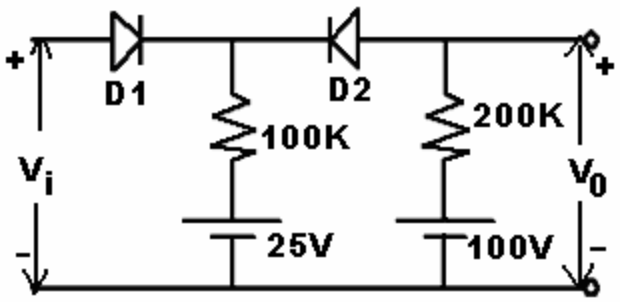

figure.2

3.a) Consider the transistor switch in CE configuration shown in figure.3, operated with V_{CC} = 12V and Vbb = 0V. It is given that $R_2 = 2R_1 = 68K\Omega$, $R_C = 2.2K\Omega$. Determine
i) The values of I_B and I_C of the transistor.
ii) The minimum value of h_{FE} required for the transistor to operate in saturation when it is in ON state?

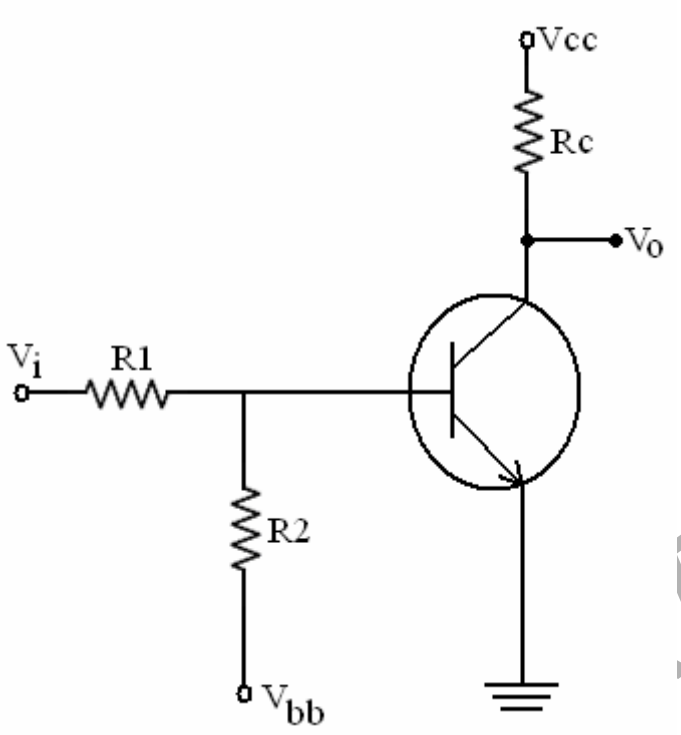

figure.3

b) Explain Zener & Avalanche breakdown mechanisms in diodes. [10+5]

4. Draw and explain the circuit of Astable Multivibrator with necessary waveforms and also derive the expression for its frequency of oscillations. [15]

5.a) What are the essential requirements of TV horizontal sweep circuit? How do you achieve them using a current sweep?

b) With neat sketches and necessary expressions, explain the transistor Miller time-base generator. [7+8]

6.a) Draw the circuit of an emitter-coupled bidirectional sampling gate and explain.

b) What is Pedestal? How pedestal can be reduced in a sampling gate circuit? [7+8]

7.a) Explain the principle of "synchronization" and 'synchronization with frequency division'.

b) Explain the method of pulse synchronization of relaxation devices, with examples. [7+8]

8.a) Realize a two-input NAND gate using Diode Transistor Logic and explain its operation with the help of truth-table.

b) Explain the terms:
i) Wired- AND connection ii) Current Source – Sink logic iii) Tri-state logic [6+9]

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1.a) Prove that for any periodic input waveform the average level of the steady state output signal from the RC high pass circuit is always Zero.
b) Draw the RC low pass circuit. With necessary waveforms and expressions explain its working for a step voltage input. [8+7]

2.a) Explain negative peak clipper with and without reference voltage.
b) Sketch the steady state output voltage for the clamper circuit shown in figure.2 and locate the output d.c level and the zero level. The diode used has R_f = 1KΩ, R_r = 600 KΩ, V_γ = 0. C = 0.1μF and R = 20 KΩ. The input is a ± 20 Volts square wave with 50% duty cycle. [5+10]

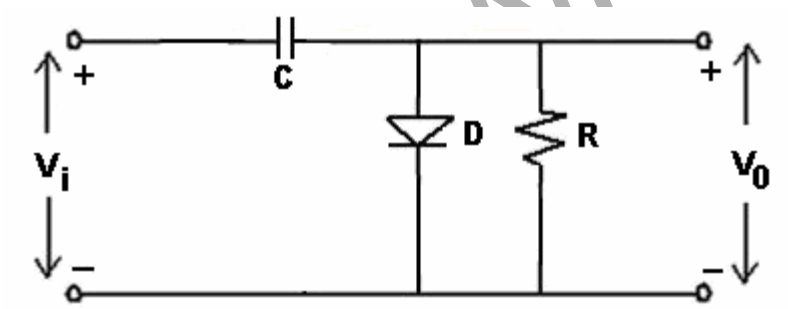

figure.2

3.a) The circuit shown in figure.3 uses a silicon transistor with h_{FE} = 100 and V_{BE} = 0.7V. Find the value of R_B which saturates the transistor, when input voltage is +5V.
Given R_C = 1K & V_{CC} = +5V.

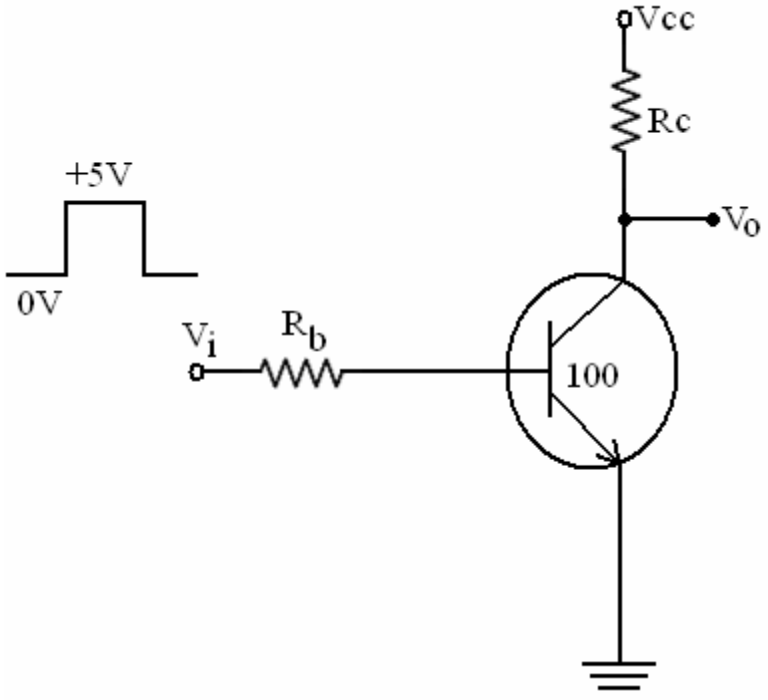

figure.3

b) Write about diode switching times. [10+5]

4. What is a monostable multivibrator? Explain with the help of a neat circuit diagram the principle of operation of a monostable multi, and derive an expression for pulse width. Draw the wave forms at collector and Bases of both transistors. [15]

5. A UJT is used as a switch across a sweep capacitor C which charges through R. A single voltage supply V_{BB} is used in the circuit. If V_V&V_P are the valley and peak voltages respectively,
a) Prove that the sweep duration is exactly given by $T_s = RC \ln (V_{BB} - V_V)/(V_{BB} - V_P)$
b) Prove that if $V_{BB} >> V_V$, then $T_S \approx RC \ln [1/(1-\eta)]$ [8+7]

6.a) Draw the circuit of FOUR-DIODE sampling gate. Derive expressions for its gain(A) and V_{min}.
b) Explain the application of sampling gate in a sampling scope. [10+5]

7.a) With neat sketches and necessary waveforms explain how an astable multivibrator can be synchronized?
b) A symmetrical astable multivibrator using transistor operates from 10V supply has a period of 1msec. Triggering pulses of spacing 750 μsec are applied to one base through a small capacitor from a high-impedance source. Find the minimum triggering pulse amplitude required to achieve 1:1 synchronization. [8+7]

8.a) Realize a three-input NAND GATE using Transistor Transistor Logic. Explain its operation with Totem-pole load.

b) With reference to logic gates, explain the terms:
i) Fan-out ii) Noise- Margin
iii) Propagation Delay iv) Figure of Merit [7+8]

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