Code No: V0423 **R07** SET - 1

**II B. Tech II Semester, Supplementary Examinations, April/May – 2013**
**SWITCHING THEORY AND LOGIC DESIGN**
(Electronics and Communications Engineering)

Time: 3 hours Max. Marks: 80

Answer any **FIVE** Questions
All Questions carry **Equal** Marks
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1. a) Perform the following conversions
   i) $(153.513)_{10}$ = ( )$_8$
   ii) $(1756.44)_8$ = ( )$_2$
   b) Encode the following numbers in Excess -3 codes.
   i) 36 ii) 678 iii) 50124
   c) Explain about error detection and correction codes.

2. a) Simplify the following Boolean expression using K-Map and implement using NAND gates only. $f(A,B,C,D) = \Sigma_m (1,2,5,6,9) + d(10,11,12,13,14,15)$
   b) Realize Ex-OR gate with minimum number of NAND gates.

3. a) Implement the following logic function using 16:1 multiplexer and 8:1 multiplexer
   $f(a,b,c,d) = \Sigma (0,3,4,8,9,15)$
   b) Draw the logic diagram of 4-bit parity generator / Checker and explain its operation.

4. a) Design a 6 bit odd/even parity generator and parity checker circuit.
   b) What is meant by two level and multilevel realization?

5. Design a PAL based adder that adds two BCD digits to give BCD sum and carry.

6. a) Design a mod-10 ripple counter using T flip flops and explain the operation.
   b) Explain the race around condition in flip flops. How this can be avoided?

7. a) Write down the steps involved in the design of finite state machines.
   b) A serial adder receives two operands A= $a_{n-1}$------$a_0$ and B=$b_{n-1}$-----$b_0$ as two sequences of bits (i=0,1,----n-1) and adds them one bit at a time to generate the sequence of bits $S_i$ of the sum as the output. Implement this serial adder as a finite state machine.

8. a) Draw the ASM chart to compare two 4-bits binary data.
   b) Name the different elements of ASM chart and discuss them.
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Code No: V0423 **R07** SET - 2

**II B. Tech II Semester, Supplementary Examinations, April/May – 2013**
**SWITCHING THEORY AND LOGIC DESIGN**
(Electronics and Communications Engineering)

Time: 3 hours Max. Marks: 80

Answer any **FIVE** Questions
All Questions carry **Equal** Marks
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1. a) Explain about error detection and correction codes.
   b) Convert the following
      i) $(27.125)_{10}$ = ( )$_8$
      ii) $(10.6875)_{10}$ = ( )$_2$
      iii) $(237.75)_8$ = ( )$_{10}$

2. a) What is meant by two level and multilevel realization?
   b) Simplify the logic function using Boolean algebra.
      F = ABC + BCD+ $\bar{A}$BC and realize using NAND gates only.

3. a) Minimize the following function and draw the circuit to realize
      $f(ABCD) = \Sigma_m(0,1,4,5,6,7,9,11,15) + \Sigma_d(10,14)$.
   b) Discuss the importance of SOP and POS forms.

4. a) Design a combinational circuit whose input is a four bit number and whose output is the 2's complement of the input number
   b) Design a BCD to decimal decoder.

5. a) Realize the switching function using PAL, $F(x_1,x_2,x_3,x_4) = \Sigma (2,3,6,7,10,12,14,15)$.
   b) Realize the following functions using PLA, $f_1=\Sigma(1,2,3,5)$, $f_2=\Sigma(2,5,6,7)$.

6. a) Explain different types of flip flops giving their truth tables.
   b) Design and draw the block diagram of a 4-bit ripple counter with the help of waveforms.

7. a) Draw the Mealy machine model of a sequential machine and discuss it.
   b) Determine the reduced flow table of the following figure.

| 00 | 01 | 11 | 10 |
|---|---|---|---|
| a,0 | b,0 | -,- | c,0 |
| -,- | b,- | e;1 | f,1 |

8. a) Differentiate between races and Hazards.
   b) Draw the ASM chart for binary multiplier.
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Code No: V0423 **R07** SET - 3

**II B. Tech II Semester, Supplementary Examinations, April/May – 2013**
**SWITCHING THEORY AND LOGIC DESIGN**
(Electronics and Communications Engineering)

Time: 3 hours Max. Marks: 80

Answer any **FIVE** Questions
All Questions carry **Equal** Marks
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1. a) Implement an EX-OR function using only NOR gates
   b) Perform the following subtraction using 1's complements.
   i) 11011 – 11001 ii) 11011 – 10011.11 iii) 1011.11 – 101.001

2. a) State and prove De-Morgan's theorems.
   b) You are presented with a set of requirement under which an insurance policy can be issued. The applicant must be
      i) A married female 25 years old or over, OR
      ii) A female under 25, OR
      iii) A married male under 25 who has not been involved in a car accident, OR
      iv) A married male who has not involved in a car accident, (OR)
      v) A married male 25 years or over who has not involved in a car accident.
   Find the algebraic expression, which assumes a value of 1 whenever the policy is issued. Simplify the expression.

3. a) What is the difference between Canonical form and Standard form? Explain.
   b) Minimize the following logic function using Tabulation method and determine the prime implicants. $f(a,b,c,d) = \Sigma_m (0,1,2,8,10,11,14,15)$.

4. a) Design a combinational circuit to convert 4-bit Gray code into binary code.
   b) Draw the circuit diagram of 8-to-1 de-multiplexer and explain the operation.

5. a) What is ROM? What size of ROM would it take to implement a binary multiplexer that multiplies two 4 bit- numbers?
   b) Derive the PLA program table for a combinational circuit that squares a 3-bit number. Minimize the number of product terms.

6. a) Design the circuit diagram of S-R latch using 2-input NOR gates.
   b) Design a 4-bit binary UP/DOWN ripple counter.

7. a) Explain in detail capabilities and limitations of finite state machines.
   b) Determine whether the function f(A,B,C,D) = ABCD+BCD is threshold function.

8. a) Differentiate between races and Hazards.
   b) Discuss the data processing and control unit of ASM chart.
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Code No: V0423 **R07** SET - 4

**II B. Tech II Semester, Supplementary Examinations, April/May – 2013**
**SWITCHING THEORY AND LOGIC DESIGN**
(Electronics and Communications Engineering)

Time: 3 hours Max. Marks: 80

Answer any **FIVE** Questions
All Questions carry **Equal** Marks
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1. a) Convert the following numbers
   i) $(1985)_{10}$ to base 8 ii) 11001010.0101 to base 10.
   b) Construct a seven-bit error correcting code augmenting the excess-3 code and by using odd 1parity check.

2. a) Minimize the function f(A,B,C,D)= ABD+$\bar{A}$CD+$\bar{A}$B+$\bar{A}$CD+ABD
   b) Draw the truth tables of NAND and NOR gates and implement them using only NAND gates.

3. a) Determine the canonical sum of products and product of sums for $\bar{A}$B+ABC+C+B.
   b) Give the procedure for simplification of a function using Tabular method.

4. a) Design a 2-bit comparator circuit using logic gates.
   b) Design and draw full adder circuit diagram using logic gates.

5. a) Realize the following functions using PLA
   $f_1$=(A,B,C) = Σ(0,2,4,5)
   $f_2$=(A,B,C)= Σ(1,5,6,7)
   b) Compare the advantages and disadvantages of PLAs with PALs.

6. a) Design a sequence detector which detects 110010. Implement the sequence detector using D-flip flops.
   b) What is twisted ring counter? How a decade counter is implemented using this counter.

7. a) The half adder takes the two data bits if start input is activated otherwise it remains in the same state. Draw the ASM chart to read the data and to store the result at different places in memory.
   b) What is the need of timing considerations in ASM charts?

8. a) Given the switching function
   $f(x_1,x_2,x_3,x_4)$= Σ (2,3,6,7,8,10,12,13,14,15). Find a minimal threshold logic realization.
   b) Describe the design procedure for asynchronous sequential circuits.
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