Code No: R22023 **R10** SET - 1

II B. Tech II Semester, Regular Examinations, April/May – 2013
SWITCHING THEORY AND LOGIC DESIGN
(Com. to EEE, ECE, ECC, BME, EIE)

Time: 3 hours Max. Marks: 75

Answer any **FIVE** Questions
All Questions carry **Equal** Marks
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1. a) Perform the binary subtraction for the following using 1's compliment method.
   i) 28-8 ii) 30-25 iii) 25.5-12.25 iv) 10.625 - 8.75
   b) Perform the following subtraction operations using 2's compliment.
   i) $(111001)_2$-$(101011)_2$ ii) $(1111)_2$-$(1010)_2$
   iii) $(112)_{10}$-$(65)_{10}$ iv) $(100.5)_{10}$-$(50.75)_{10}$ (7M+8M)

2. a) Find the compliments of the following
   i) xy'+x'y ii) (AB'+C)D'+E iii) (ABC)'(A+B+C) iv) AB'C+A'BC+ABC
   b) Simplify the following algebra expressions
   i) x'+y'+xyz' ii) A+A'B+A'B'C+A'B'C'D
   iii) BC+C'D'+ABD' iv) w'x'+x'y'+x'z'+yz (7M+8M)

3. Simplify the following Boolean function by using tabulation method.
   $F(A,B,C,D) = \Sigma_m(0,1,2,5,7,8,9,10,13,15)$ (15M)

4. a) Implement Full adder circuit using ROM and verify the working.
   b) Design a half adder and subtractor using suitable gates. (8M+7M)

5. a) Implement the following functions using a decoder.
   $f_1(x,y,z) = \Sigma_m(0,1,3,7)$
   $f_2(x,y,z) = \Sigma_m(2,3,7)$
   b) Design a full subtractor circuit with decoder. (8M+7M)
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6. a) Draw and explain the block diagram of PLA.
   b) Implement the following Boolean functions using PAL
   $F_1(x,y,z) = \sum (0,2,12,13)$ $F_2(x,y,z) = \sum(0,2,6,8,9,12,13)$
   $F_3(x,y,z) = \sum (0,2,9,10,12,13)$ $F_4(x,y,z) = \sum (1,3,4,6,12,14)$ (7M+8M)

7. a) Compare synchronous and Asynchronous circuits.
   b) Design a Mod-6 synchronous counter using J-K flip flops. (8M+7M)

8. a) Distinguish between Mealy and Moore machines.
   b) Convert the following Mealy machine into a corresponding Moore machine. (7M+8M)

PS	NS,Z	
	X-0	X=1
A	B,0	E,0
B	E,0	D,0
C	D,1	A,0
D	C,1	E,0
E	B,0	D,0

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1. a) The binary numbers listed have a sign bit in the left most position and, if negative numbers are in 2's complement form. Perform the arithmetic operations indicated and verify the answers.
   i) 101011 + 111000 ii) 001110 + 110010
   iii) 111001 – 001010 iv) 101011 – 100110
   b) Perform the following subtraction operations using 9's and 10's complements
   i) 83-25 ii) 37-69 iii) 56.25-17.12 (8M+7M)

2. a) Simplify the expressions
   i) AB+AB'(A'C')' ii) AB+A(B+C)+B(B+C)
   iii) $f = \Sigma_m(1,3,5,7)$ iv) $f=\Pi_M(3,5,7)$
   b) Simplify the following to least number of literals by manipulation of Boolean algebra.
   i) AB'C'D+A'B'D+BCD'+A'B+BC' ii) ABC+A'B+ABC'
   iii) x + xyz + x'yz + xw + xw' + x'y iv) (x+y+z) (x+y) x (7M+8M)

3. Simplify the following expressions using K-map
   a) A'B+ABD+AB'CD'+BC b) ABC+A'B'C+A'BC+ABC'+A'B'C'
   c) AB+AC'+AD+AB'C+ABC (15M)

4. a) Realize Full Adder Using two half adders and logic gates.
   b) Draw the block diagram of BCD adder using two 4-bit parallel binary adders and logic gates. (5M+10M)

5. a) Implement the following function using 8×1 multiplexer: $F = \sum(0,1,5,7)$
   b) Implement a full adder using decoder. (8M+7M)
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6. List the PLA programming table and draw the PLA structure for the BCD-to-excess-3 code converter. (15M)

7. a) Find a modulo-6 gray code using k-Map & design the corresponding counter.
   b) Distinguish between asynchronous and synchronous sequential circuit. (8M+7M)

8. For the given minimal state - table:
   a) Give proper assignment.
   b) And design the circuit using D - Flip-flops. (8M+7M)

Present State q^v	Next state, q^{v+1}		out - put Z	
	X=0	X=1	X=0	X =1
q_1	q_2	q_1	0	0
q_2	q_3	q_1	0	0
q_3	q_4	q_5	0	0
q_4	q_4	q_1	0	0
q_5	q_2	q_1	1	0

Code No: R22023 **R10** SET - 3

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Time: 3 hours Max. Marks: 75

Answer any **FIVE** Questions
All Questions carry **Equal** Marks
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1. a) Convert the following to Decimal and then to Binary.
   i) 1876_{16} ii) $AB22_{16}$ iii) 1212_8 iv) 1556_8 v) 977_{10}
   b) Perform subtraction with the following unsigned decimal numbers by taking 10's complement of the subtrahend. Verify the result.
   i) 5250- 1321 ii). 1753 – 8640 (9M+6M)

2. a) Reduce the following Boolean expression to the indicated number of literals
   i) A'C'+ABC+AC' to three literals ii) (x'y'+z)'+z+xy+wz to three literals
   b) Convert the given expressions into SOP form.
   i) (x+z)(x'+y)(y+z) ii) (A'+B'+C')(A+B'+C) (7M+8M)

3. Simplify the following Boolean functions using K-map
   a) $f(A,B,C,D,E) = \sum_m (0,2,3,4,6,7,9,11,16,18,19,20,22,23,25,27)$
   b) $f(A,B,C,D,E) = \sum_m (0,4,7,8,9,10,11,16,24,25,26,27,29,31)$ (7M+8M)

4. a) Design a circuit to convert Excess-3 code to BCD code using a 4-bit Full adder.
   b) Design a full subtractor using gates? (8M+7M)

5. a) Explain the terms Multiplexing and Demultiplexing
   b) Realize the function using (i) 8:1 MUX (ii) 4:1 MUX for the function
   $f(A,B,C,D) = \sum_m (0,3,4,7,9,13,15)$ (7M+8M)

6. Tabulate the PLA programming table for the four Boolean functions: A(x,y,z) = ∑ (1,2,4,6), B(x,y,z) = ∑(0,1,6,7), C(x,y,z) = ∑ (2,6), D(x,y,z) = ∑ (1,2,3,5,7) Minimize the number of product terms and also show the internal logic in the PLA structure. (15M)

7. a) Draw and explain 4-bit universal shift register.
   b) Explain different types of shift registers. (7M+8M)

8. A clocked sequential circuit is provided with a single input x and single output Z. Whenever the input produce a string of pulses 1 1 1 or 0 0 0 and at the end of the sequence it produce an output Z = 1 and overlapping is also allowed.
   a) Obtain State - Diagram. b) Also obtain state - Table. (3M+4M+8M)
   c) Find equivalence classes using partition method & design the circuit using D flip-flops.
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Time: 3 hours Max. Marks: 75

Answer any **FIVE** Questions
All Questions carry **Equal** Marks
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1. a) Convert the following to Decimal and then to octal.
   i) 257_{16} ii) 199_{16} iii) 10110001_2 iv) 11001100_2 v) 344_{10}
   b) Convert the following to Decimal and then to Octal.
   i) 101100012 ii) 110011002 (9M+6M)

2. a) Generate Hamming code for the given 11 bit message 10101110101 and rewrite the entire message with Hamming code
   b) Simplify the following Boolean expression to a minimum number of literals. (7M+8M)
   i) x'y'+xy+x'yii) (x+y) (x+y') iii) x'+xy+xz'+xy'z' iv) x'yz+xz

3. Simplify the following Boolean function by using tabulation method and verify the same with K-map minimization.
   $f(A,B,C,D) = \sum_m (0,2,3,6,7,8,10,12,13)$ (15M)

4. a) Design a full adder using AND & OR gates?
   b) Explain the operation of carry look-a-head adder? (8M+7M)

5. a) List out the applications of multiplexer.
   b) Realize the function $f(A,B,C,D) = \prod (1,4,6,10,14) + d(0,8,11,15)$ using
   i) 16×1 MUX ii) 8×1 MUX iii) 4×1 MUX (5M+10M)
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6. a) Derive the PLA programming table for the combinational circuit that squares a 3 bit number.
   b) For the given 3-input, 4-output truth table of a combinations circuit, tabulate the PAL programming table for the circuit.

Inputs			Output			
x	y	z	A	B	C	D
0	0	0	0	1	0	0
0	0	1	1	1	1	1
0	1	0	1	0	1	1
0	1	1	0	1	0	1
1	0	0	1	0	1	0
1	0	1	0	0	0	1
1	1	0	1	1	1	0
1	1	1	0	1	1	1

(7M+8M)

7. a) Explain synchronous and ripple counters. Compare their merits and demerits.
   b) Design a modulo -12 up synchronous counter using T- flip flops and draw the circuit diagram. (7M+8M)

8. a) Explain the capabilities and limitations finite state machine.
   b) For the machine given below, find the equivalence partition and the corresponding reduced machine in standard form.

P.S	N.S, Z	
	x=0	X=1
A	E,0	C,0
B	C,0	A,0
C	B,0	G,0
D	G,0	A,0
E	F,1	B,0
F	E,0	D,0
G	D,0	G,0

(5M+10M)