Code No: X0224 **R07** SET - 1

II B. Tech I Semester, Supplementary Examinations, Nov – 2012
SWITCHING THEORY AND LOGIC DESIGN
(Com. to EEE, EIE, BME, ECC)

Time: 3 hours Max. Marks: 80

Answer any **FIVE** Questions
All Questions carry **Equal** Marks
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1. a) Convert $(0011101.1011)_2$ to decimal
   b) Represent the 12 bit Hamming code word for the 8 bit data words 10110110 and 10101100
   c) Draw a conversion table to convert BCD to Gray code (4M+6M+6M)

2. a) Explain the fundamental postulates of Boolean algebra
   b) Obtain the compliment and dual for the following expressions
   i) AB' + ABD +ABD'+A'C'D' + A'BC'C ii) BD +BCD'+ A'B'C'D' (8M+8M)

3. a) Simplify the following Boolean function F using k maps and implement the circuit using NAND gates only F= ∑m(5,6,7,10,11,13,14,15)
   b) Express the simplified Boolean function in sum of min terms.
   i) F(x,y,z)=∑(0,2,6,11,12,13,14) ii) F(x,y,z)=∑(0,1,3,5,6,8,9,11,12,13) (8M+8M)

4. a) Design a 64X1 multiplexer with four 16X1 and one 4X1 multiplexers.
   b) Explain 3 to 8 line decoder with the help of logic diagram and truth table (8M+8M)

5. Realize the following functions using a PLA with 6 inputs, 4outputs and 10 AND gates
   i) F(A,B,C,D,E,F) = ∑m(0,1,2,3,7,8,9,10,11,15,32,33,34,35,39,40,41,42,43,45,47).
   ii) F(A,B,C,D,E,F) = ∑m(8,9,10,11,12,14,21,25,27,40,41,42,43,44,46,57,59). (8M+8M)

6. a) Design a modulo 12 counter using a shift register and feedback logic.
   b) A 5 stage ripple counter uses flip flops having a delay time of 30 ns and a decode time of 50 ns. Determine the maximum frequency of operation of the counter. (8M+8M)
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7. a) Describe the procedure to reduce the state table.
   b) Convert the following Mealy machine into the corresponding Moore machine (6M+10M)

PS	NS,Z	
	X=0	X=1
A	B,0	E,0
B	D,0	A,1
C	D,1	A,0
D	B,1	C,1
E	A,0	A,0

8. a) Design a digital system with three 4-bit registers A, B and C to perform the following operations by drawing the ASM chart.
   i) Transfer two binary numbers to A and B when a start signal is enabled.
   ii) If A<B shift left the contents of A and transfer the result to register C
   iii) If A>B shift right the contents of B and transfer the result to register C
   iv) If A=B transfer the number to register C unchanged.
   b) Realize the above using JK flip flops and D flip flops. (8M+8M)

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1. a) Convert the following decimal numbers to octal numbers
   i) 6987 ii) 9351.25
   b) Convert the following numbers to Gray code
   i) 6482 ii) 754
   c) What is self complementary code? Explain . (6M+6M+4M)

2. a) Find the compliment and dual of
   i) $F = AB + \overline{C}D + \overline{E}$ ii) $F = A\overline{B}C + B + B\overline{D} + AB\overline{D} + \overline{A}C$
   b) Minimize the functions Y = AB + A(B+C) + B(B+C) and Y = (AB + C) (B +AC) using Boolean theorems. (8M+8M)

3. Minimize the following function using tabular minimization and verify the same with K-map minimization F=∑(0,2,4,6,9,13,21,23,25,29,31) (16M)

4. Implement the following Boolean function by a hazard free OR-AND network f = ∑m(0,2,6,7) and explain in detail what are the hazards encountered in implementing the above function (16M)

5. a) Tabulate the PLA programming table for the two Boolean functions listed below
   i) A(x,y,z) = ∑m(1,23,5,7) ii) B(x,y,z) = ∑m(0,1,6,7)
   b) Give the logic implementation of a 32X4 bit ROM using decoder of suitable size. (8M+8M)

6. a) Draw and explain Master-Slave D flip flop.
   b) Explain SR flip flop with the help of NAND gates and also obtain its excitation table
   c) Discuss about Race-around condition (6M+6M+4M)
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7. a) Distinguish between Moore and Mealy machines.
   b) For the state table of the machine given below find the equivalent partition and corresponding reduced machine in standard form (4M+12M)

PS	NS,Z	
	X=0	X=1
A	B,1	H,1
B	F,1	D,1
C	D,0	E,1
D	C,1	F,1
E	D,1	C,1
F	C,1	C,1
G	C,1	D,1
H	C,0	A,1

8. Draw the ASM chart of binary multiplier and design the control circuit using each of the following methods:
   i) JK flip flop & gates ii) D flip flop& decoder.. (8M+8M)

Code No: X0224 **R07** SET - 3

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1. a) Design single error correcting Hamming code for standard BCD and explain how error is detected and corrected.
   b) Subtract the following numbers using 10's and 9's complement
      i) 7642-428 ii) 527-309. (8M+8M)

2. a) Realize a 2 input EX-OR gate using minimum number of 2 input NAND gates
   b) Implement the Boolean function $F = \overline{A}B + \overline{A}B\overline{C} + \overline{A}B\overline{C}\overline{D}E$ with exclusive OR and AND gates. (8M+8M)

3. Minimize the following function using tabular minimization and verify the same with K-map minimization F=∑(1,4,6,7,8,9,10,11,15) (16M)

4. a) Realize the function F = ∑m(0,1,4,7,9,12,14) using 1:16 de-Mux.
   b) What is meant by hazard in combinational circuit? How do you design hazard free circuit explain with suitable example. (8M+8M)

5. a) Realize the following Boolean functions using Threshold gate
      i) F = ∑m(0,3,5,6,8,9,14,15) ii) F = ∑m(1,2,5,11,12,13,14,15).
   b) Write short notes on PLA (12M+4M)

6. a) Design a modulo-7 binary counter using JK flip flop.
   b) Mention the applications of flip flops.
   c) A ripple counter uses flip flops having tpd = 12 ns. What can be the largest mode counter constructed from flip flops and operated at 10MHz frequency (8M+4M+4M)
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7. a) What is a merger graph? Explain.
   b) For the state table of the machine given below, find the equivalent partition and a corresponding reduced machine in standard form. (4M+12M)

PS	NS,Z	
	X=0	X=1
A	D,0	H,1
B	F,1	C,1
C	D,0	F,1
D	C,0	E,1
E	C,1	D,1
F	D,1	D,1
G	D,1	C,1
H	B,1	A,1

8. a) Differentiate between an ASM chart and a conventional flow chart.
   b) Draw the state diagram and ASM chart of a J-K flip-flop. (8M+8M)

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1. a) Convert the numbers to octal and decimal number system
   i) $(A50C)_{16}$ ii) $(1101011.0110)_2$
   b) Explain error correction and detection codes with examples (8M+8M)

2. a) Simplify the following Boolean expressions
   i) $\overline{A}\,\overline{C} + ABC + A\overline{C}$
   ii) $\overline{(\overline{X}\ \overline{Y}\ Z)} + Z + XY + WZ$
   iii) $\overline{A}\left(B\left(\overline{D} + \overline{C}D\right)\right) + B\left(A + \overline{A}CD\right)$
   iv) $\left(\overline{A} + C\right)\left(\overline{A} + \overline{C}\right)\left(A + B + \overline{C}D\right)$
   b) Briefly describe about the standard form and canonical form of switching functions with suitable examples. (8M+8M)

3. Obtain minimal SOP expression for the given Boolean function, using K-map method
   F = $\sum$ (0,1,4,6,8,9,10,12) + d(3,7,11,13,14,15) and draw the circuit using 2 input NAND gates. (16M)

4. What are hazards? Explain in detail significance of hazards. Differentiate between static and dynamic hazards. (16M)

5. a) Implement the following Boolean functions using PROM
   i) P(A,B,C,D) = $\sum$m(0,2,6,7,8,9,12,13,14)
   ii) Q(A,B,C,D) = $\sum$m(1,3,4,6,9,12,14)
   b) Write short notes on i) PLA ii) PLD (8M+8M)

6. a) With the aid of external logic convert D type flip flop to a JK flip flop.
   b) Design a synchronous modulo 12 counter using NAND gates and JK flip flops (8M+8M)
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7. a) Draw the state stable for a synchronous circuit, with one input x and one output z, which operates according to the following sequences at t = 0, the initial state is A and
$x(t) = 0$ for $t < 0$
i) $z(t) = x(t) + x(t-1)$ ii) $z(t) = x(t).x(t-1)$
where the change from equation(i) to equation(ii) occurs at time such that
$x(\tau) = x(t-\tau) = x(\tau-2) = 1$ and change from (ii) to (i) occurs at time T such that $x(T) = X(T-1) = X(T-2) = 0$
b) Define successor and terminal state (10M+6M)

8. a) Name the elements of an ASM chart and define each one of them.
b) Draw the state diagram, state table and ASM chart for a D flip-flop. (8M+8M)