Code No: V0423 **R07** SET - 1

II B. Tech II Semester, Supplementary Examinations, Dec – 2012
SWITCHING THEORY AND LOGIC DESIGN
(Electronics and Communications Engineering)

Time: 3 hours Max. Marks: 80

Answer any **FIVE** Questions
All Questions carry **Equal** Marks
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1. a) Convert the given Gray code number to equivalent binary 1001001011110010.
   b) Convert $(A0F9.0EB)_{16}$ to decimal, binary, and octal.

2. a) Simplify the following Boolean expressions using the Boolean theorems.
   i) (A+B+C) (B'+C) + (A+D) (A'+C) ii) (A+B) (A+B') (A'+B)
   b) Why a NAND and NOR gates are known as universal gates? Realize all the basic gates using NAND and NOR

3. a) Minimize the following expressions using K-map and realize using NAND Gates.
   $f = \sum m (1, 3, 5, 8, 9, 11, 15) + d (2, 13)$
   b) Minimize the following expression using K-map and realize using NOR Gates.
   $f = \prod M (1, 2, 3, 8, 9, 10, 11, 15). d (7, 1, 5)$

4. a) Describe the operations performed by the following logic circuits with an example
   i) Comparator ii) Decoder iii) Encoder
   b) Explain the operation of a 3-to-8 decoder 74LS138. Realize 4-to-16 decoder using two 3-to-8 decoders.

5. a) Is an X-OR function a threshold function? Justify.
   b) Realize the following function using a PROM of size 8x3 $F = \sum m(1,2,4,6)$

6. a) Explain the differences between asynchronous and synchronous counters. Design a MOD-10 ripple counter.
   b) Design and construct MOD-5 synchronous counter using JK flip flops.

7. a) What are the Moore and Melay machines? Compare them.
   b) Explain the procedure for state minimization using the partition technique.

8. a) Name the elements of an ASM chart and define each one of them.
   b) Explain the control subsystem implementation of weighing machine.
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Code No: V0423 **R07** SET - 2

II B. Tech II Semester, Supplementary Examinations, Dec – 2012
SWITCHING THEORY AND LOGIC DESIGN
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Time: 3 hours Max. Marks: 80

Answer any **FIVE** Questions
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1. a) Solve for x
   i) $(367)_8=(x)_2$ ii) $(378.93)_{10}=(x)_8$ iii) $(B9F.AE)_{16}=(x)_8$ iv) $(16)_{10}=(100)_x$
   b) Convert $(163.875)_{10}$ to binary, octal, hexadecimal.

2. a) Obtain dual of the following Boolean expressions
   i) AB+A(B+C)+B'(B+D) ii) A+B+A'B'C.
   b) Obtain the compliment of the following Boolean expressions
   i) A'B+A'BC'+A'BCD+A'BC'D'E. ii) ABEF+ABE'F'+A'B'EF.

3. a) Minimize the following expression using K-map and realize using NAND Gates.
   $F(A,B,C,D) = \sum m(0,1,2,9,11) + d(8,10,14,15)$.
   b) Minimize the following expression using K-map and realize using NOR gates.
   $f = \prod M(0,4,6,7,8,12,13,14,15)$

4. a) Explain the differences between a MUX and a DEMUX. Realize 16-input multiplexer by cascading of two 8-input multiplexers 74151.
   b) Realize the function $f(A,B,C,D) = \prod(1,4,6,10,14) + d(0,8,11,15)$ using
   i) 16:1 MUX ii) 8:1 MUX

5. a) Give the comparison between PROM, PLA and PAL.
   b) Implement the following Boolean function with PLA $F(A,B,C) = \sum m(0,1,2,4)$

6. a) What is a shift register? Explain about the following modes of operations in a four bit shift register i) shift right ii) shift left iii) bidirectional.
   b) Explain the differences between ring and Johnson counters. Design and explain the operation of a decade Johnson counter.

7. a) What are the capabilities and limitations of finite state machines?
   b) Explain the procedure for state minimization using merger graph and merger table.

8. a) Differentiate between an ASM chart and a conventional flow chart.
   b) Explain in detail the ASM technique of designing a sequential circuit.
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Code No: V0423 **R07** SET - 3

II B. Tech II Semester, Supplementary Examinations, Dec – 2012
SWITCHING THEORY AND LOGIC DESIGN
(Electronics and Communications Engineering)

Time: 3 hours Max. Marks: 80

Answer any **FIVE** Questions
All Questions carry **Equal** Marks
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1. a) Solve for x
   i) $(257)_8 = (x)_2$ ii) $(21.625)_{10} = (x)_8$ iii) $(BC.2)_{16} = (x)_8$ iv) $(33)_{10} = (201)_x$
   b) Express the Decimal Digits 0-9 in BCD, 2421, 84-2-1 and Excess-3.

2. a) Prove the following Boolean theorems
   i) AB+A'C = (A+C)(A'+B) ii) AB+A'C+BC = AB+A'C
   b) Simplify the following Boolean expressions
   i) ABC+AB'+ABC' ii) ACD+A'BCD.

3. a) Minimize the following expressions using K-map and realize using NAND Gates.
   $f = \sum m(0,1,4,5,6,7,9,11,15) + d(10,14)$
   b) Minimize the following expression using K-map and realize using NOR Gates.
   $f = \prod M(1,4,5,11,12,14) \cdot d(6,7,15)$

4. a) Implement full adder with 4 to 1 multiplexer.
   b) Implement 64 x 1 multiplexer with four 16 x 1 and one 4 x 1 multiplexer.

5. a) Give the logic implementation of a32x4 bit ROM using decoder of suitable size.
   b) Implement the following Boolean function with PLA $F(A,B,C) = \sum m(1,5,6,7)$

6. a) Draw and explain 4-bit universal shift register.
   b) Explain the differences between asynchronous and synchronous counters. Design a MOD-6 ripple counter.

7. a) What are the Moore and Melay machines? Compare them.
   b) Explain the procedure for state minimization using merger graph and merger table.

8. a) Draw and explain ASM chart for a weighing machine.
   b) Explain in detail about salient features of ASM chart.
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Code No: V0423 **R07** SET - 4

II B. Tech II Semester, Supplementary Examinations, Dec – 2012
SWITCHING THEORY AND LOGIC DESIGN
(Electronics and Communications Engineering)

Time: 3 hours Max. Marks: 80

Answer any **FIVE** Questions
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1. a) Covert 105.15_{10} to binary, octal, hexadecimal.
   b) what is hamming code? How is the hamming code word tested and corrected.

2. a) State and prove i) commutative, ii) associative, iii) distributive, iv) idempotence, v) distributive laws of Boolean algebra.
   b) State and prove i) consensus theorem, ii) transposition theorem, iii)De-Morgan's theorem.

3. Minimize the following expressions using K-map and realize using NAND Gates.
   $f = \sum m(5,6,7,9,10,11,13,14,15)$
   $f = \sum m(0,1,4,5,6,7,9,11,15) + d(10,14)$

4. a) Explain the differences between a MUX and a DEMUX. Realize 16-input multiplexer by cascading of two 8-input multiplexers 74151.
   b) Realize the function $f(A,B,C,D) = \sum m(1,2,5,8,10,14) + d(6,7,15)$ using
   i) 16:1 MUX ii) 8:1 MUX iii) 4:1 MUX.

5. a) Explain steps to implement a Boolean function using threshold gate.
   b) Write the program table to implement a BCD to XS-3 code conversion using PLA.

6. a) Explain the operation of R-S master slave flip flop. Explain its truth table
   b) Explain about the realization of SR flip-flop, JK flip-flop using D flip-flop.

7. a) What are the capabilities and limitations of finite state machines?
   b) Explain the procedure for state minimization using the partition technique.

8. a) Draw and explain the ASM chart for a binary multiplier.
   b) Explain the data path subsystem for a weighing machine.
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