Code No: R22023 **R10** SET - 1

II B. Tech II Semester, Supplementary Examinations, Dec – 2012
SWITCHING THEORY LOGIC DESIGN
(Com. to EEE, ECE, ECC, BME, EIE)

Time: 3 hours Max. Marks: 75

Answer any **FIVE** Questions
All Questions carry **Equal** Marks
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1. a) Convert the following numbers
   i) $(2568)_{10}$ to base 6 ii) $(A87)_{12}$ to base 10
   b) If A = -37 and B = +19 Represent A and B in 8-bit 2's complement.
   ii) Find A+B ii) Find A-B (8M+7M)

2. a) Consider the message bits m_4 m_3 m_2 m_1 = 1101. Encode it into Hamming code to detect single error.
   b) Obtain the compliment and dual for the following expressions
   i) AB + BC + AC ii) A+B'C(A+B+C') iii) AB+(AC)'+(AB+C) (6M+9M)

3. Simplify the following Boolean function F; then express the simplified Boolean function in sum of minterms.
   i) $F(x,y,z)=\sum(1,3,5,6,11,13)$ ii) $F(x,y,z)=\sum(0,1,2,8,10,14,15)$ (7M+8M)

4. a) Design a Full adder circuit with AND, OR, NOT gates.
   b) Explain Excess-3 adder circuit with an example. (5M+10M)

5. a) Design a BCD to decimal decoder.
   b) Design 8X1 multiplexer using 2X1 multiplexers
   c) Differentiate between encoder and priority encoder. (4M+7M+4M)

6. a) Design a BCD to excess-3 code converter using
   i) ROM ii)PAL
   b) Write short notes on Multi-gate synthesis. (8M+7M)

7. a) Design a Mod-6 synchronous counter using JK flip flops.
   b) Draw and explain the working of Master-Slave JK flip flop. (7M+8M)

8. a) What are the capabilities and limitations of Final State Machines?
   b) A clocked sequential circuit is provided with a single input X and single output Y. whenever the input produce string of pulses 1 1 1 or 0 0 0 and at end of the sequence it produces an output Y = 1 and overlapping is also allowed. Find equivalence classes using partition method and design the circuit using D flip flops (4M+11M)
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Code No: R22023 **R10** SET - 2

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1. a) Represent the unsigned decimal numbers 975 and 357 in BCD, and then show the necessary steps to find their sum.
   b) What is a self complementary code? Explain with two examples. (8M+7M)

2. a) Design a logic circuit having three inputs A, B, C such that output is 1 when A = 0 or whenever B = C = 1. Also obtain logic circuit using NAND gates.
   b) Given AB'+ A'B=C show that AC'+A'C=B. (8M+7M)

3. Minimize the following function using tabular minimization and verify the same with K-map minimization F=∑(2,4,9,10,11,12,19,20,21,22,23,24,25,26,29,31) (15M)

4. a) Generate 2's compliment for the given 4 bit number using Full adders.
   b) Write short notes on BCD adder circuit (8M+7M)

5. a) Construct a 4 to 16 line decoder with five 2 to 4 line decoders with enable.
   b) Show how BCD ripple counter can be implemented. (7M+8M)

6. a) Give the comparison between PROM, PLA and PAL.
   b) Determine whether the X-OR function is a threshold function. Justify.
   c) Write short notes on PLA. (6M+5M+4M)

7. a) Distinguish between combinational and sequential logic circuits.
   b) Convert a D flip flop into
      i) SR flip flop ii) JK flip flop iii) T flip flop. (6M+9M)

8. a) Explain in detail the Mealy state diagram and ASM chart for it with an example.
   b) Show that 8 exit paths in an ASM block emanating from the decision boxes that check the eight possible binary values of three control variables. (7M+8M)
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Answer any **FIVE** Questions
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1. a) Explain different methods used to represent negative numbers in binary system.
   b) In a new number system X and Y are successive digits such that $(XY)_r = (25)_{10}$ and $(YX)_r = (31)_{10}$. Find X,Y,r (6M+9M)

2. a) Explain the fundamental postulates of Boolean algebra
   b) Implement the Boolean function F= AB' CD' + A' BCD' + A B'C'D + A BC'D with exclusive OR and AND gates. (6M+9M)

3. Minimize the following function using tabular minimization and verify the same with K-map minimization F=∑(0,2,4,5,6,7,8,10,14,17,18,21,29,31) +∑d(11,20,22) (15M)

4. a) Implement a Full subtractor with two half subtractors and an OR gate.
   b) Write short notes on look-ahead adder circuit. (8M+7M)

5. a) Design an excess-2 to BCD code converter using a 4-bit full adders MSI circuit.
   b) Design 64 line output de-multiplexer using 4 to 16 and 2 to 4 de-multiplexers (7M+8M)

6. a) Implement the following Boolean functions with a PLA
   i) F (x,y,z) = ∑ (0,1,2,4) ii) F (x,y,z) = ∑ (0,5,6,7)
   b) Implement Full adder circuit using ROM (10M+5M)

7. a) Define a sequential system and explain how it differs from a combinational system..
   b) Draw the circuit of 4 bit Johnson counter using D flip flops and explain its operation with the help of bit pattern. (6M+9M)

8. a) What are the capabilities and limitations of finite state.
   b) For the state table of the machine given below, find the equivalent partition and a corresponding reduced machine in standard form. (7M+8M)

PS	NS,Z	
	X=0	X=1
A	B,1	H,1
B	F,1	D,1
C	D,0	E,1
D	C,1	F,1
E	D,1	C,1
F	C,1	C,1
G	C,1	D,1
H	C,0	A,1
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Code No: R22023 **R10** SET - 4

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1. a) Convert the decimal number 508.75 to base 7, 8 and 12
   b) Represent the decimal number 7258 in
   i) BCD code ii) excess-3 code iii)2421 code iv) 6311 code (7M+8M)

2. a) Explain error correction and error detection codes with examples.
   b) Implement the following Boolean function F using the two-level form
   i) NAND-AND ii) AND-NOR where F (A,B,C,D) =∑(0,1,2,3,4,8,9,12) (7M+8M)

3. Simplify the following using K-map method and tabulation method
   F(A,B,C,D,E)=∑(0,2,4,9,13,21,23,25,29,31) (15M)

4. a) Design a Full adder using half adders and carry look ahead adders.
   b) Mention the applications of Full adders. (11M+4M)

5. a) Design 3 to 8 line decoder circuit using NOR gates only.
   b) What is meant by hazard in combinational circuit (12M+3M)

6. A combinational circuit is defined by the functions:
   F_1 (A,B,C) = ∑ m (3,5,6,7)
   F_2 (A,B,C) = ∑ m(0,2,4,7). Implement the circuit with a PLA having three inputs, four product terms and two outputs. (15M)

7. a) Design a modulo-12 up synchronous counter using T- flip flops and draw the circuit diagram.
   b) Explain synchronous and ripple counters. Compare their merits and demerits. (9M+6M)

8. a) The output Z of a fundamental mode, two input sequential circuit is to change from 0 to 1 only when x_2 changes from 0 to 1 while $x_1 = 1$. The output changes from 1 to 0 only when x_1 changes from 1 to 0 while $x_2 = 1$. Find a minimum row reduced table.
   b) Draw the state diagrams of a sequence detector which can detect 011. (8M+7M)
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