Code: R7210204

R07

B.Tech II Year I Semester (R07) Supplementary Examinations, May 2013

SWITCHING THEORY & LOGIC DESIGN

(Common to EEE, EIE, E.Con.E & ECC)

Time: 3 hours Max. Marks: 80

Answer any FIVE questions

All questions carry equal marks

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1 (a) (i) Convert $(1126.148)_{10}$ to hexadecimal.
(ii) Convert $(10011.1101)_2$ to decimal.
(iii) Convert $(11001111.01101001)_2$ to octal.
(iv) Convert $(789.0123)_8$ to binary.
(b) Explain, how error occurred in a data transmission can be detected using parity bit.

2 (a) Implement the INVERTER gate, OR gate and AND gate using NAND gate, NOR gate.
(b) Determine the canonical sum-of-products representation of the function:
$f(x, y, z) = z + (x' + y)(x + y')$.

3 (a) Let 'F' be a function for which the product of all true prime implicants is 0. Prove that F cannot be linearly separable.
(b) Simplify using K-map F (A, B, C, D, E) = $\sum$ (0, 4, 8, 12, 18, 20, 26, 28).

4 (a) Design a 2 to 4 decoder using NAND gates.
(b) Explain how decoder acts as a demultiplexer.

5 (a) Discuss about threshold logic. Briefly explain the capabilities and limitations of threshold gate.
(b) Write a brief note on programmable logic devices.

6 (a) Design a basic flip-flop and explain its operation.
(b) Design a 8-bit ring counter.

7 (a) Explain the minimization procedure of completely specified sequential machines.
(b) Explain about FSM in detail with an example.

8 (a) Differentiate conventional flow chart and algorithmic state machine chart.
(b) Give the procedure to design a data processing unit and a control unit.

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