Code: 9A04401

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B.Tech II Year II Semester (R09) Regular & Supplementary Examinations, April/May 2013

SWITCHING THEORY AND LOGIC DESIGN

(Common to EEE, EIE, E.Con.E, ECE and ECC)

Time: 3 hours Max Marks: 70

Answer any FIVE questions

All questions carry equal marks

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1 (a) Distinguish between weighted and non-weighted codes with examples.

(b) Represent the decimal number 8620 in: (i) BCD (ii) XS3 (iii) Gray codes

2 (a) What are universal gates? Realize AND, OR, NOT, XOR gates using universal gates.

(b) Given Boolean expression AB' + A'B = C. Show that AC' + A'C = B.

(c) Prove that OR-AND network is equivalent to NOR-NOR network.

3 (a) What are the advantages of tabulation method over K-map?

(b) Simplify the following Boolean function using tabulation method.
Y(A,B,C,D) = ∑(1,3,5,8,9,11,15)

4 Design BCD to XS3 code converter and realize using logic gates.

5 (a) The following memory units are specified by the no of words times the number of bits per word. How many address lines and input-output data lines are needed in each case? (i) 5K × 16 (ii) 3G × 8 (iii) 32M × 32 (iv) 256K × 64.

(b) Give the number of bytes stored in the memories listed above.

6 (a) Distinguish between a state table and a flow table.

(b) Draw the logic diagram and write functional table of an SR latch using NAND gates. Explain the operation.

7 (a) Define state equivalence and machine equivalence with reference to sequential machines.

(b) A clocked sequential circuit with single input and single output Z is defined by the following D - flip-flop input equations and output equations of Z.

$$D_1 = \overline{Q_1}Q_2\overline{Q_3}x$$
$$D_2 = Q_1\overline{Q_2Q_3}$$
$$D_3 = \overline{Q_1Q_3}\overline{x} + \overline{Q_1}Q_3\overline{x}$$
$$Z = Q_1Q_2Q_3x$$

(i) Obtain state table.

(ii) Draw the state diagram.

8 Draw the state diagram for mod-6 counter and obtain ASM chart.

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1 (a) Why 8421 BCD code is widely used in computers?

(b) What are the rules for 8421 BCD addition? Add the two decimal numbers 7546 and 3462 in 8421 code.

(c) Distinguish between weighted and non-weighted codes with examples.

2 (a) State duality theorem. List Boolean laws and their duals.

(b) Simplify the following Boolean functions to minimum number of literals.
(i) F = ABC + ABC' + A'B. (ii) F = (A+B)' (A'+B').

(c) Realize XOR gate using minimum number of NAND gates.

3 (a) List the Boolean function simplification rules using tabulation method.

(b) Simplify the following Boolean function using tabulation method.
$Y(A, B, C, D) = \sum(0, 1, 2, 3, 5, 7, 8, 9, 11, 14)$

4 (a) Implement full adder using decoder and OR gates.

(b) Realize the Boolean function $T(X, Y, Z) = \sum(1, 3, 4, 5)$ using logic gates for hazard free.

5 (a) Design a combinational circuit using ROM that accepts 3-bit number and generates output binary number equal to the square of the input number.

(b) Write short notes on types of read only memory.

6 (a) Design a serial binary adder using D-Flip Flop.

(b) Draw the circuit diagram of J-K Flip-Flop with NAND gates with positive edge triggering and explain its operation with the help of truth table. How race around condition is eliminated?

7 Define:
(i) Finite state machine.
(ii) State equivalence and machine minimization.
(iii) Distinguishable states and sequence.

8 Design a half adder and half subtractor circuit using multiplexer.

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1 (a) Explain error detection codes.
(b) What is the drawback of error detection codes?
(c) Construct even parity 7 bit hamming code for the message 0100.

2 (a) Draw the symbols and truth tables of all logic gates and explain.
(b) Simplify the following Boolean functions to minimum number of literals.
(i) xy + y'z' + wxz' (ii) w'x' + x'y' + w'z' + yz
(c) Realize XOR gate using minimum number of NAND gates.

3 (a) Define prime implicant and essential prime implicant with example using K-map.
(b) Find all the prime implicants for the following Boolean function using K-map and determine which are essential.
$F(A,B,C,D) = \sum(1,3,4,5,9,10,11,12,13,14,15)$

4 Design a combinational circuit that converts a decimal digit from 8, 4,-2,-1 code to 8,4,2,1 BCD code.

5 (a) Find the minimal threshold-logic realization for the function:
$f(A, B, C, D) = \Sigma m (2, 3, 6, 7, 10, 12, 14, 15)$
(b) Compare programmable logic devices.

6 (a) Design a mod-6 asynchronous counter using T-flip flop.
(b) Compare synchronous and asynchronous sequential circuits.

7 A clocked sequential circuit is provided with a single input x and single output z. Whenever the input produce a string of pulses 1 1 1 or 0 0 0 and at the end of the sequence it produce an output z = 1 and overlapping is also allowed.
(a) Obtain state diagram.
(b) Also obtain state table.
(c) Find equivalence classes using partition method.

8 (a) Write short notes on ASM chart.
(b) Draw the state diagram for a full adder and convert it to ASM chart and realize the circuit.

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4

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Time: 3 hours Max Marks: 70

Answer any FIVE questions

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1 (a) Explain the method of error detection in binary codes.

(b) Construct the BCD code with even parity and odd parity bit for decimal 0 to 9.

(c) Construct 7 bit hamming code for data1001. Use even parity.

2 (a) State duality theorem. List Boolean laws and their duals.

(b) Simplify the following Boolean functions to minimum number of literals.

(i) xy + xy' (ii) (x + y)(x + y')

(c) Realize XOR gate using minimum number of NAND gates.

3 (a) Draw 3-variable and 4-variable K-map and define pair, quad and octet.

(b) Simplify the following Boolean function for minimal POS form using K-map and implement using NOR gates.

F(W, X, Y, Z) = ∑(1, 2, 5, 6, 9) + d(10, 11, 12, 13, 14, 15)

4 (a) Design 4-bit even parity generator. Mention truth table.

(b) Design BCD to XS3 code converter using a 4-bit full- adders MSI circuit.

5 (a) Design a combinational circuit using PROM that converts a 3-bit binary number to equivalent excess-3 code.

(b) Write short notes on threshold logic.

6 (a) Convert SR-flip-flop into JK-flip-flop.

(b) Compare sequential and combinational circuits.

7 A Clocked sequential circuit with two inputs x and y and a single output z is defined by the following J - K flip-flops state equations and output equation of z.

$$Q_1^+ = Q_1\overline{x} + Q_1 y + Q_2 x + \overline{Q_1 Q_2 \overline{y}}$$
$$Q_2^+ = \overline{Q_1} Q_2 \overline{x} + \overline{Q_1} Q_2 y + \overline{Q_1 Q_2 x}$$
$$Z = (Q_1 + Q_2)\overline{xy}$$

Where Q+1, ξQ+2 are the next states and Q1, ξQ2 are the present states of JK flip-flops. (a) Obtain state table. (b) Obtain state diagram.

8 (a) Explain in detail the block diagram of ASM chart.

(b) Draw the portion of an ASM chart that specifies the conditional operation to increment register R during state T_1 and transfer to state T_2, if control inputs z and y are = 1 and 0 respectively.

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