Code No: N1021/R07 **Set No. 1**

IV B.Tech I Semester Supplementary Examinations, Feb/Mar 2011
VLSI DESIGN
(Common to Electronics & Instrumentation Engineering and Electronics & Computer Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. With neat sketches explain BICMOS fabrication process in an N well. [16]
2. (a) Explain briefly about MOS transistor switch.
   (b) Discuss the square law model of FET. [8+8]
3. Discuss the following with examples with reference to VLSI design
   (a) Design hierarchy
   (b) Regularity. [8+8]
4. (a) Define and explain the following:
      i. Sheet resistance concept applied to MOS transistors and inverters.
      ii. Standard unit of capacitance.
   (b) Explain the requirement and functioning of a delay unit. [4+4+8]
5. (a) How can the components of CMOS system design be categorized into the groups.
   (b) Why is the static 6 transistor cell used for average CMOS system design?
   (c) Compare the performance of CMOS Off chip and On chip memory designs. [4+6+6]
6. Draw the structure, explain the function and write the applications characteristics of the following programmable CMOS devices: [16]
   (a) PLA
   (b) PAL
   (c) FPGA
   (d) CPLD.
7. (a) Write a VHDL program for 7-sengment display decoder.
   (b) What are the basic sources of errors in CMOS circuits and how these are tested? Give name of such a simulator. [8+8]
8. (a) What is ATPG? Explain a method of generation of test vector.
   (b) Explain the terms controllability, observability and fault coverage. [8+8]

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Code No: N1021/R07 **Set No. 2**

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Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
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1. (a) Clearly explain the diffusion process in IC fabrication.
   (b) Clearly explain various diffusion effects in silicon with emphasis on VLSI application. [8+8]
2. (a) Derive the nMOS inverter transfer characteristics.
   (b) Explain the possibility of using a CMOS inverter as an amplifier. [8+8]
3. (a) what is a stick diagram? Draw the stick diagram and layout for a CMOS inverter.
   (b) What are the effects of scaling on V_t?
   (c) What are design rules? Why is metal- metal spacing larger than poly -poly spacing. [8+4+4]
4. Describe the constructional features and performance characteristics of the following.
   (a) Pseudo - n MOS logic.
   (b) Clocked - C MOS logic. [8+8]
5. (a) Explain the CMOS system design based on the I/O cells with suitable example.
   (b) Design a four bit parity generator using only XOR gates and draw the Schematic of it. [8+8]
6. (a) What are the differences between a gate array chip and standard-cell chip? What benefits does each implementation style have?
   (b) Write the equations for a full adder in SOP form. Sketch a 3-input, 2- output PLA implementing this logic. [8+8]
7. (a) Compare the Concurrent signal assignments, sequential signal assignments and process statements.
   (b) Why resettable registers are preferable and what is the difference between Synchronous and Asynchronous resets? [8+8]
8. (a) Explain the manufacturing test of a chip with suitable examples.
   (b) Explain how an Ad-hoc test technique used to test long counters. [8+8]

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Code No: N1021/R07 **Set No. 3**

IV B.Tech I Semester Supplementary Examinations, Feb/Mar 2011
VLSI DESIGN
(Common to Electronics & Instrumentation Engineering and Electronics & Computer Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Compare CMOS and Bipolar technologies.
   (b) With neat sketches explain nMOS fabrication process. [8+8]
2. (a) Differentiate between the transfer characteristic of nMOS depletion inverter and nMOS enhancement inverters.
   (b) Describe n MOS transistor circuit model. [8+8]
3. (a) what is a stick diagram? Draw the stick diagram and layout for a CMOS inverter.
   (b) What are the effects of scaling on V_t?
   (c) What are design rules? Why is metal- metal spacing larger than poly -poly spacing. [8+4+4]
4. Describe three sources of wiring capacitances. Explain the effect of wiring capacitance on the performance of a VLSI circuit. [16]
5. (a) Draw the schematic for Transmission gate adder and explain its operation with truth table.
   (b) Show the basic one row and one column RAM architecture and explain its operation. [8+8]
6. (a) Draw the diagram of programmed I/O pad and explain how the antifuses are used in this.
   (b) Draw and explain the AND/OR representation of PLA. [8+8]
7. (a) Write a architecture for a 4- bit Counter in both behavioral and structural styles.
   (b) Explain with example how mixed mode simulator are more for CMOS circuits testing. [8+8]
8. (a) Draw the basic structure of parallel scan and explain how it reduces the long scan chains.
   (b) Draw the state diagram of TAP Controller and explain how it provides the control signals for test data and instruction register. [8+8]

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Code No: N1021/R07 **Set No. 4**

IV B.Tech I Semester Supplementary Examinations, Feb/Mar 2011
VLSI DESIGN
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Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. Describe in detail encapsulation process in IC fabrication. [16]
2. (a) Derive an equation for I_{ds} of an n channel enhancement MOSFET operating in saturation region.
   (b) An n MOS transistor is operating in saturation region with the following parameters.V_{gs}=5V, V_{tn} =1.2V, (W/L) =10: $\mu_n c_{ox}$=110μA/V^2. Find transconductance of the device. [8+8]
3. (a) what is a stick diagram? Draw the stick diagram and layout for a CMOS inverter.
   (b) What are the effects of scaling on V_t?
   (c) What are design rules? Why is metal- metal spacing larger than poly -poly spacing. [8+4+4]
4. Explain
   (a) Propagation delay
   (b) Wiring capacitance. [8+8]
5. (a) Draw and explain the Booth decode cell used for Booth multiplier.
   (b) Compare different types of CMOS subsystem shifters. [8+8]
6. (a) Compare the Antifuse and Vialink programmable interconnections for PAL devices.
   (b) What are different typically available SSI Standard-cell types and compare them. [8+8]
7. (a) What is the importance of operator precedence in VHDL? Is the AND operation takes place before OR operation?
   (b) What is mean by Hierarchy in VHDL? Write a program for 4 input multiplexer from 2 input multiplexers. [8+8]
8. (a) What are the reasons of malfunctioning of chip? What are the different levels of testing?
   (b) Explain how a parallel scan is used for data path test.
   (c) What is mean by level sensitive of logic system? [6+6+4]

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