Code No: R32045 **R10** **Set No: 1**

III B.Tech. II Semester Regular Examinations, April/May -2013

VLSI DESIGN

(Comm to Electronics and Communication Engineering & Electronics and Computer Engineering & Electronics and Instrumentation Engineering)

Time: 3 Hours **Max Marks: 75**

Answer any FIVE Questions

All Questions carry equal marks

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1. (a) Explain the structure PMOS Enhancement Transistor
   (b) Discuss the steps involved in P – well CMOS process

2. Derive an expression for MOS transistor threshold voltage

3. (a) What is the need for Stick diagrams?
   (b) Draw and explain about stick diagram of CMOS 3 – input NOR gate.

4. Discuss about following MOS Capacitances
   (i) MOS Structure Capacitances (ii) Channel Capacitance
   (ii) Junction Capacitance (iv) Capacitive devise Model

5. (a) What are the objectives of scaling in VLSI Technology?
   (b) Draw and explain the structure of scaled MOS transistor.

6. (a) Discuss about structure of CPLD's.
   (b) Discuss about Full Custom Design.

7. (a) Discuss about VLSI circuit design process using HDL's.
   (b) Compare VHDL and Verilog HDL.

8. Discuss the VHDL structural description of 4- bit adder.

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Code No: R32045 **R10** **Set No: 2**

III B.Tech. II Semester Regular Examinations, April/May -2013

VLSI DESIGN

(Comm to Electronics and Communication Engineering & Electronics and Computer Engineering & Electronics and Instrumentation Engineering)

Time: 3 Hours **Max Marks: 75**

Answer any FIVE Questions

All Questions carry equal marks

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1. (a) Explain the structure NMOS Enhancement Transistor
   (b) Discuss the steps involved in N – well CMOS process

2. Derive an equation for relation of drain current and gate to source voltage and drain to source voltage for NMOS transistor.

3. (a) What is the need for design rules and layout?
   (b) Draw and explain about stick diagram of CMOS 3 – input NAND gate.

4. (a) Discuss about MOS transistor threshold voltage variation with respect to channel length and drain to source voltage.
   (b) Discuss about Fan-in and Fan out characteristics MOS circuits.

5. Discuss the effect of scaling on following device parameters.
   (i) Gate area (ii) Gate Capacitance (iii) Parasitic capacitance
   (iv) Carrier Density in Channel (v) Channel Resistance (vi) Gate Delay
   (vii) Max Operating Frequency

6. (a) Draw and explain NMOS NAND- NAND PLA realization.
   (b) Discuss about Semi Custom Design.

7. (a) Discuss the concept Hardware simulation.
   (b) Explain about levels of abstractions of VHDL.

8. (a) Write a D Flip – Flop model in VHDL and discuss.
   (b) Discuss about technology libraries in VHDL.

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Code No: R32045 **R10** **Set No: 3**

III B.Tech. II Semester Regular Examinations, April/May -2013

VLSI DESIGN

(Comm to Electronics and Communication Engineering & Electronics and Computer Engineering & Electronics and Instrumentation Engineering)

Time: 3 Hours **Max Marks: 75**

Answer any FIVE Questions

All Questions carry equal marks

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1. (a) Explain the structure PMOS Depletion Transistor.
   (b) Discuss the steps involved in Twin Tub CMOS process.

2. (a) Explain channel length modulation of NMOS transistor.
   (b) Discuss about Bi CMOS inverter.

3. (a) Discuss about Lambda based design rules.
   (b) Draw and explain about stick diagram of CMOS 2 – input NOR gate.

4. Derive expressions for CMOS inverter delays.

5. Discuss the effect of scaling on following device parameters
   (i) Saturation Drain Current (ii) Current density (iii) Switching energy per gate
   (iv) Power Dissipation per Gate (v) Power dissipation per unit area
   (vi) Power speed Product

6. (a) Draw and explain NMOS NOR-NOR PLA realization.
   (b) Discuss about usefulness of FPGA's.

7. (a) Discuss the concept Hardware Synthesis.
   (b) Explain the usage of subprograms in VHDL.

8. (a) Write a J-K Flip – Flop model in VHDL and discuss
   (b) Discuss about functional gate level verification

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Code No: R32045 **R10** **Set No: 4**

III B.Tech. II Semester Regular Examinations, April/May -2013

VLSI DESIGN

(Comm to Electronics and Communication Engineering & Electronics and Computer Engineering & Electronics and Instrumentation Engineering)

Time: 3 Hours **Max Marks: 75**

Answer any FIVE Questions

All Questions carry equal marks

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1. (a) Explain the structure PMOS Depletion Transistor.
   (b) Compare CMOS and Bipolar technologies.

2. (a) Discuss Latch-up in CMOS and Bi-CMOS circuits.
   (b) Explain MOS transistor Figure of Merit.

3. (a) Discuss about double metal MOS process rules.
   (b) Draw and explain about stick diagram of CMOS 2 – input NAND gate.

4. Realize 3 – input NAND and NOR gates using NMOS, PMOS and CMOS transistors and explain them with logic.

5. Discuss the limitations of scaling in VLSI Technology in detail.

6. (a) Draw the basic PLA structure and discuss about it.
   (b) Discuss about Gate Arrays.

7. (a) Discuss the requirements of VHDL.
   (b) Discuss about packages and bindings in VHDL.

8. (a) Give a model of 4 to 1 multiplexer in VHDL and explain.
   (b) Discuss about post lay out simulation.

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