Code No: V3219 **R07** **Set No: 1**

III B.Tech. II Semester Supplementary Examinations, April/May - 2013

VLSI DESIGN

(Common to EEE, ECE, BME)

Time: 3 Hours **Max Marks: 80**

Answer any FIVE Questions

All Questions carry equal marks

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1. a) Explain clearly about Moore's law.
   b) What is the need of VLSI circuits?
   c) Draw typical VLSI design in Y chart representation and explain.

2. Explain clearly about different operating regions in CMOS inverter transfer characteristics with neat diagrams.

3. Realize function 'F' by CMOS logic, draw the stick diagram and layout diagram for $F = (ABC)^1$.

4. a) Describe three sources of wiring capacitances.
   b) Explain the effect of wiring capacitance on the performance of a VLSI circuit.

5. a) Explain the CMOS system design based on the I/O cells with suitable example.
   b) Design a four bit parity generator using only XOR gates and draw the Schematic of it.

6. a) Draw the typical standard-cell structure showing regular-power cell and explain it.
   b) Draw and explain the pseudo-nMOS PLA schematic for full adder and what are the advantages and disadvantages of it.

7. a) Explain how VHDL is developed and where it was used initially?
   b) What are the different design capture tools? Explain them briefly.

8. a) Why the chip testing is needed? At what levels testing a chip can occur?
   b) What is the drawback of serial scan? How to overcome this?

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Code No: V3219 **R07** **Set No: 2**

III B.Tech. II Semester Supplementary Examinations, April/May - 2013

VLSI DESIGN

(Common to EEE, ECE, BME)

Time: 3 Hours **Max Marks: 80**

Answer any FIVE Questions

All Questions carry equal marks

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1. a) List out the processing steps involved in the manufacturing of an IC.
   b) With neat sketches explain BICMOS fabrication process.

2. a) Define $g_{m,}$ $r_{ds,}$ and figure out merit of MOS transistor.
   b) Draw transfer characteristics of CMOS inverter and describe.

3. Design a stick diagram for the 3-input N MOS logic and Draw the circuit diagram and layout for it.

4. a) Draw and explain fan in and fan out characteristics of different CMOS design technologies.
   b) What are the alternate gate circuits available? Explain any one of item with suitable sketch.

5. Explain briefly the CMOS system design based on the data path operators, memory elements, control structures and I/O cells with suitable examples.

6. a) Draw a self timed dynamic PLA and what are the advantages of it compared to footed dynamic PLA.
   b) Explain the tradeoffs between using a transmission gate or a tristate buffer to implement an FPGA routing block.

7. a) Compare the Hardware and Software Languages.
   b) Draw the basic design flow through typical CMOS VLSI tools and give some names of corresponding tools.

8. a) Explain the gate level and function level of testing.
   b) What is sequential fault grading? Explain how it is analyzed.

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Code No: V3219 **R07** **Set No: 3**

III B.Tech. II Semester Supplementary Examinations, April/May - 2013

VLSI DESIGN

(Common to EEE, ECE, BME)

Time: 3 Hours **Max Marks: 80**

Answer any FIVE Questions

All Questions carry equal marks

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1. Briefly discuss the steps involved in the manufacturing process of an IC.

2. a) Draw and explain the characteristics of nMOS transistor in different modes of operation and its body effect.
   b) Give the design aspects and draw the circuit diagram of nMOS inverter and with the help of transfer characteristics.

3. What is the purpose of design rule? What is the purpose of stick diagram? What are the different approaches for describing the design rule? Give three approaches for making contacts between poly silicon and discussion in NMOS circuit.

4. a) Discuss about area capacitances of MOS layers and give area capacitance calculations with suitable examples.
   b) Illustrate driving large capacitive loads with relevant examples.

5. a) Draw the top level schematic and a floor plan for 16 × 16 Booth recoded multiplier and explain its operation.
   b) Explain the tradeoffs between open, closed, and twisted bit lines in a dynamic RAM array.

6. a) Draw and explain the Anti fuse Structure for programming the PAL device.
   b) Explain how the I/O pad is programmed in FPGA.

7. a) Write a architecture for a 4- bit Counter in both behavioural and structural styles.
   b) Explain with example how mixed mode simulator is more for CMOS circuits testing.

8. a) A sequential circuit with ‘n’ inputs and ‘m’ storage devices. To test this circuit how many test vectors are required?
   b) What is sequential fault grading? Explain how it is analyzed.

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Code No: V3219 **R07** **Set No: 4**

III B.Tech. II Semester Supplementary Examinations, April/May - 2013

VLSI DESIGN

(Common to EEE, ECE, BME)

Time: 3 Hours **Max Marks: 80**

Answer any FIVE Questions

All Questions carry equal marks

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1. a) With neat sketch explain fabrication process of P-well CMOS Processes.
   b) What is Lithography, & what are the Lithography techniques used in IC technology.

2. Compare the relative merits of three different forms of pull up for an inverter circuits. What is the best choice for realization in
   a) nMOS technology b) CMOS technology? and explain.

3. a) Discuss in detail the NMOS design style.
   b) Discuss CMOS design style. Compare with NMOS design style.

4. a) What is a transmission gate? Explain clearly about it. Draw the symbols of transmission gate.
   b) Implement XOR gate using transmission gate.

5. a) Draw the schematic for tiny XOR gate and explain its operation.
   b) Draw the circuit diagram for 4-by-4 barrel shifter using complementary transmission gates and explain its shifting operation.

6. a) What are different classes of Programmable CMOS devices? Explain them briefly.
   b) What is the basis for standard-cell? What are basic classes of circuits for Library cells?

7. Write a syntax for the following in VHDL :
   a) If b) Case c) When d) generic e) Entity

8. Briefly explain about
   a) Chip level test techniques
   b) System level test techniques

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