Code: R7411001

R07

B.Tech IV Year I Semester (R07) Supplementary Examinations, May 2013

**VLSI DESIGN**

(Common to EIE and ECC)

Time: 3 hours Max. Marks: 80

Answer any FIVE questions

All questions carry equal marks

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1 (a) Write in brief about integrated passive components.
(b) With neat sketches, explain BICMOS fabrication process in an N well.

2 (a) With neat sketches, explain the transfer characteristic of a CMOS inverter.
(b) Derive an equation for Ids of an n-channel enhancement MOSFET operating in saturation region.

3 (a) Write the scaling factors for different types of device parameters.
(b) Discuss the limits due to sub threshold currents.

4 (a) Explain clocked CMOS logic, domino logic and n-p CMOS logic.
(b) In gate logic, compare the geometry aspects between two-inputs NMOS NAND and CMOS NAND gates.

5 (a) Draw the top level schematic and a floor plan for 16 X 16 booth recoded multiplier and explain its operation.
(b) Explain the tradeoffs between open, closed and twisted bit lines in a dynamic RAM array.

6 (a) Draw a self timed dynamic PLA and what are the advantages of it compared to foot dynamic PLA.
(b) Explain the tradeoffs between using a transmission gate or a tri-state buffer to implement an FPGA routing block.

7 (a) Explain how VHDL is developed and where it was used initially.
(b) What are the different design capture tools? Explain them briefly.

8 (a) Explain how function of system can be tested.
(b) Explain any one of the method of testing bridge faults.
(c) What type of faults can be reduced by improving layout design?

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